SQ7705
Brief Datasheet V1.2

SQ7705, 16-bit Low Power Secure MCU
64K Bytes Flash, 8K Bytes EEPROM, 8K Bytes SRAM, ADC, AES, SHA, Secure Boot

Features

- Max. System Frequency 48 MHz
- Instruction Set is Compatible with Toshiba TLCS-870/C1
- Operating Voltage: 2.0V ~ 5.5V
- Operating Temperature: -40°C ~ 85°C
- Deep Sleep Mode Current < 1uA

Memory Configuration

- SRAM 8K Bytes
- Flash 64K Bytes (512bytes / sector)
- EEPROM 8K Bytes (32bytes / sector)
- EEPROM and Code Flash support dual operation

Low voltage detection (LVD) system

Brown-out reset detection (BROR)

Clock Source

- External High Frequency Crystal : 1~16 MHz
- External Low Frequency Crystal : 32.768 KHz
- System Frequency Up to 48MHz (via PLL)
- Internal Low Frequency Oscillator: 32KHz

Timer/Counter

- Three 16-bit Timer (TCA), with timer mode, external trigger timer mode, pulse width measurement mode, PPG mode.
- Six 8/16-bit Timer(Timer A), complementary PWM output with dead time
- Real-time Clock (RTC)
- Time Base Timer (TBT)
- Watchdog Timer (WDT)
- System Timer (STM)
- Divider Output (DVO)

I/O

- 53 I/O for 64pin Package
- 8 external interrupt input (EINT0~EINT7)
- 16 Key-on Wakeup (KWI0~KWI 15)

Package Type

- LQFP 64 (10x10)
- QFN 40 (5x5)

12-bit ADC

- 16 CH ADC input
- ADC Vref

DMA

- 4CH for Performance Demanding Applications

Peripherals

- 1 set Low Energy UART
- 3 sets UART
- 2 sets I2C   (max. 400KHz)
- 2 sets SPI   (max. 10MHz)

Hardware Accelerated Symmetric Crypto Engine

- SHA2-256 Hash Engine
- AES-128/AES-256 (ECB, CBC, CFB, CTR, OFB) with Side Channel Attack Countermeasures
- Up to 2.9Mbps hardware AES engine which is useful for real-time voice and audio encrypt/decrypt

NIST CAVP Certified Cryptographic Algorithms

- DRBG (SP800-90A)
- TRNG (SP800-22 Compliant)
- AES-128/AES-256 (FIPS 197)
- SHA-256 (FIPS 180-4)

Hardware-isolated, Secure Execution Environment

- Support Secure Zone and Secure Peripherals
- Support Secure Bootloader and Anti-Tamper
- Secure Memory (SRAM, Flash, EEPROM)

NIST FIPS 140-3 compliant tamper-resistant technology

Applications

- Smart Home, Smart Lock,
- BMS System
- Wireless Node Device
- IoT Application

1. Preface

SQ7705 has a maximum operating frequency of 48MHz, has 64KB Flash, 8KB EEPROM, 8KB SRAM, supporting secure storage. Providing hardware AES-128/AES-256 and SHA-256 engines, and side-channel attack protection and tamper detection. It has a 12-bit ADC, high-precision internal high-frequency oscillator (±1.5%, -20~70℃) and precise low-voltage detection (LVD), and consumes <1.2uA in deep sleep mode. Rich peripherals: 3 16-bit timers (with counter, external trigger, PWM, PPG), 3 8/16-bit timers (with dead-zone complementary PWM output), 3 sets of UART, 1 set of low-power UART, 2 sets of I2C, 2 sets of SPI, RTC with perpetual calendar function, wake-up and interrupt functions. With a variety of internal and external clock sources, users can optimize and adjust the working mode according to different needs such as performance and power consumption.

SQ7705 uses the 870E core and is compatible with the TLCS-870/C1 instruction set architecture. It is a power-efficient and low-gate-count computing core. Its variable-length instruction set provides 38 sets of core instructions, 9 addressing modes, and the instruction opcode length. From 1 to 5 digits, most general instructions are 2 to 4 digits.

The core is a three-stage pipeline design. The instruction queue and core functional units can frequently execute instructions in a single cycle. The Harvard architecture allows the system to fetch instructions and access data at the same time. Specific hardware is specially designed to handle instruction and data alignment to improve work efficiency.

A variety of internal and external clock sources can be selected according to the frequency required by the user, and can also support digital peripherals and precise analog features. Users can optimize and adjust the working mode according to different needs such as performance and power consumption.

Note: In 8KB EEPROM, 7.5K Bytes are for customer configuration; 0.5K Bytes are for MCU internal use.

Product No.	SQ7705LA064SGGR	SQ7705N5040SGGR
Pins/ (IOs)	64 / (53)	40/ (53)
Operating Voltage	2.0~5.5V	2.0~5.5V
Operating Temp.	-40~85°C	-40~85°C
External Interrupt	16	16
Flash	64K Bytes	64K Bytes
EEPROM	8K Bytes	8K Bytes
RAM	8K Bytes	8K Bytes
ADC	12-bit x16-CH (VDD, External)	12-bit x16-CH (VDD, External)
Interrupt	External : 8 Internal : 44	External : 8 Internal : 44
Internal Oscillator / Accuracy	48MHz +/- 1% @　0~50°C +/- 1.5% @ -20~70°C +/-　3% @ -40~85°C	48MHz +/- 1% @　0~50°C +/- 1.5% @ -20~70°C +/-　3% @ -40~85°C
External Crystal	1~16MHz ,32768Hz	1~16MHz ,32768Hz
BROR	1 Level	1 Level
LVD	8 Levels (+/- 3%)[*2]	8 Levels (+/- 3%)[*2]
Timer / Counter	8/16-bit Timer A x 3	8/16-bit Timer A x 3
	16-bit TCA x 3	16-bit TCA x 3
	WDT,TBT,RTC,STM	WDT,TBT,RTC,STM
PWM/PPG	8/16-bit Timer A x 3	8/16-bit Timer A x 3
	16-bit TCA x 3	16-bit TCA x 3
Communication	LEUART x 1 UART x 3 SPI x 2 I2C x 2	LEUART x 1 UART x 3 SPI x 2 I2C x 2
OCDE	Yes	Yes
Package Type	LQFP64(10x10)	QFN40(5x5)

Note 1:" VDD" means using VDD as internal reference voltage; "external" means there is on external reference voltage

Note 2: SQ series products have 8-level LVD, with a minimum accuracy of ±3%. For detailed specifications of each level, please refer to the product specification sheet.
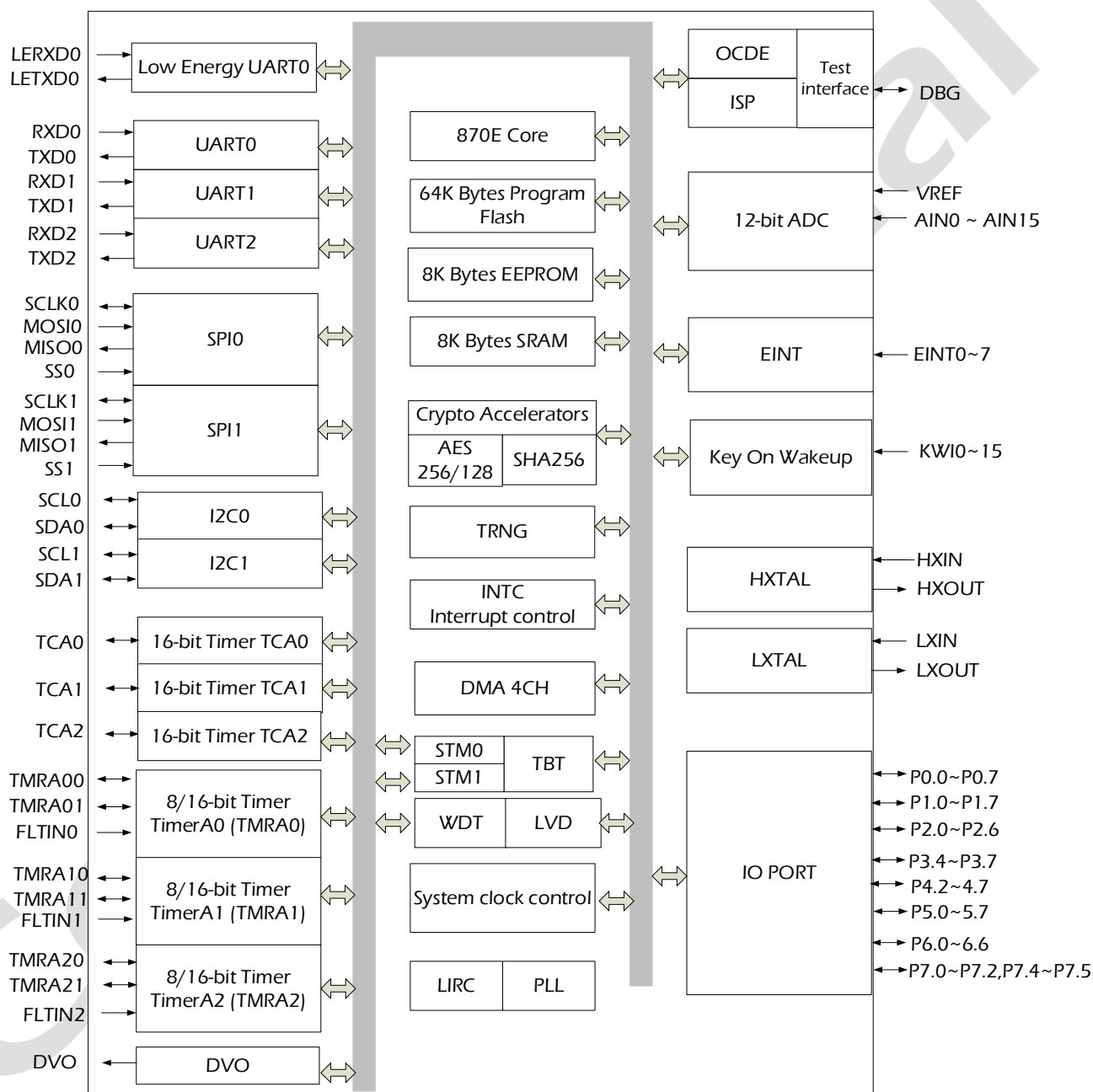
2. Product Overview

2.1 Block Diagram

Figure 2-1 SQ7705 Block Diagram

Note : TimerA (TMRA) is 8/16-bit timer/counter；TMRA00 and TMRA01 are timer/counter input/output function.

2.2 Pin Assignment/ Description
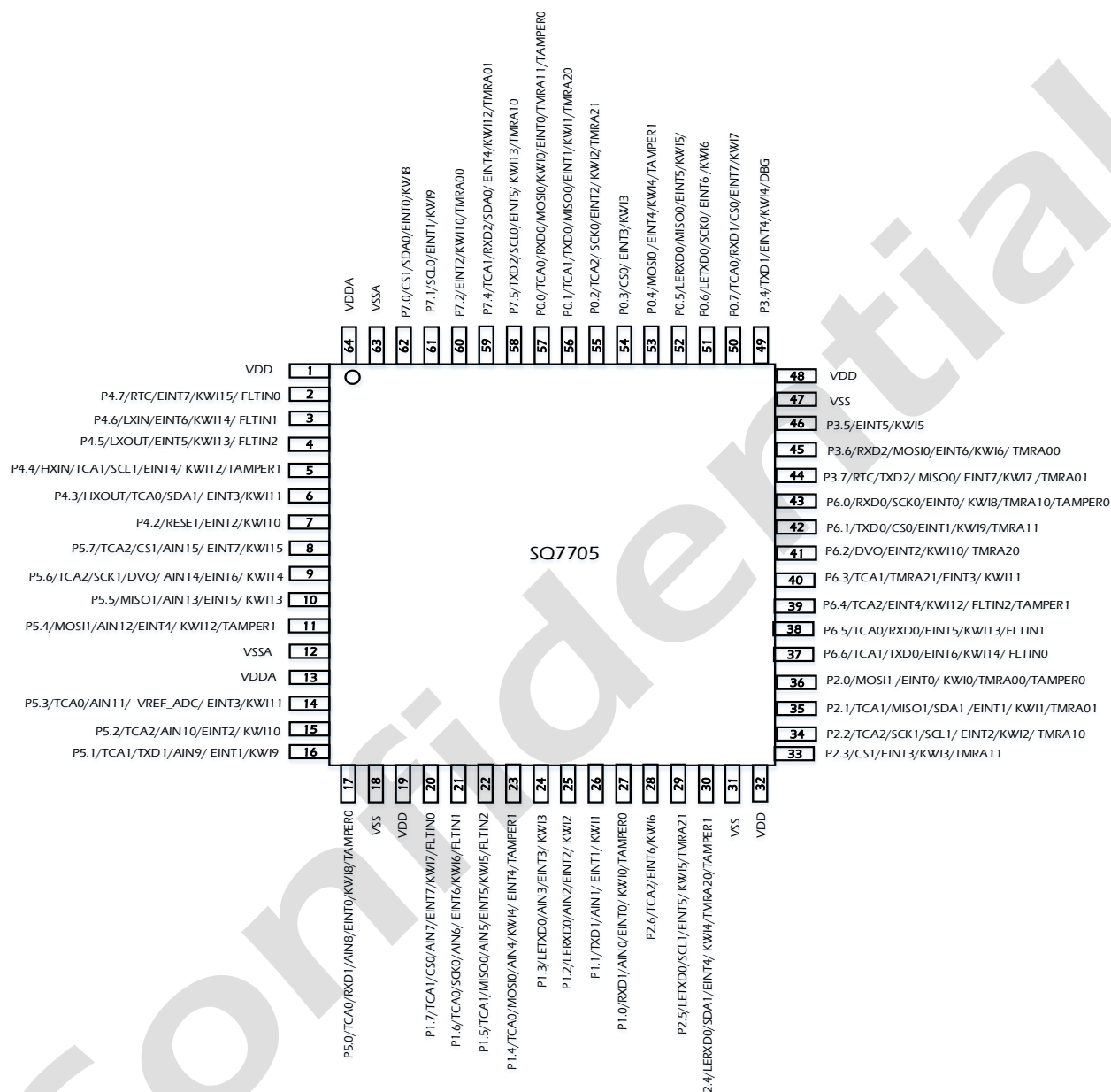
Product No.: SQ7705LA064SGGR (LQFP64 10x10)

Figure 2-2 Pin Assignment of SQ7705 (LQFP-64)

Note 1: SQ7705 simulation needs to connect P3.4/DBG, P4.2/RESET, VDD, and VSS. For the simulation pins reserved by the customer on the system board, please refer to the external reference circuit. It is not recommended to add other components to avoid affecting the simulation characteristics or functions

Note 2: SQ7705 programming is performed by OCDE pins. For the programming pins reserved by the customer on the system board, please refer to the external reference circuit. It is not recommended to add other components to avoid affecting the programming characteristics or Function. 4-wire OCDE pin: Same as the simulation pin (P3.4/DBG, P4.2/RESET, VDD, and VSS). It takes about (7) seconds to burn the 64KByte program space in a single IC. iMQ emulator (MQ-Link) and writer support this burning mode.
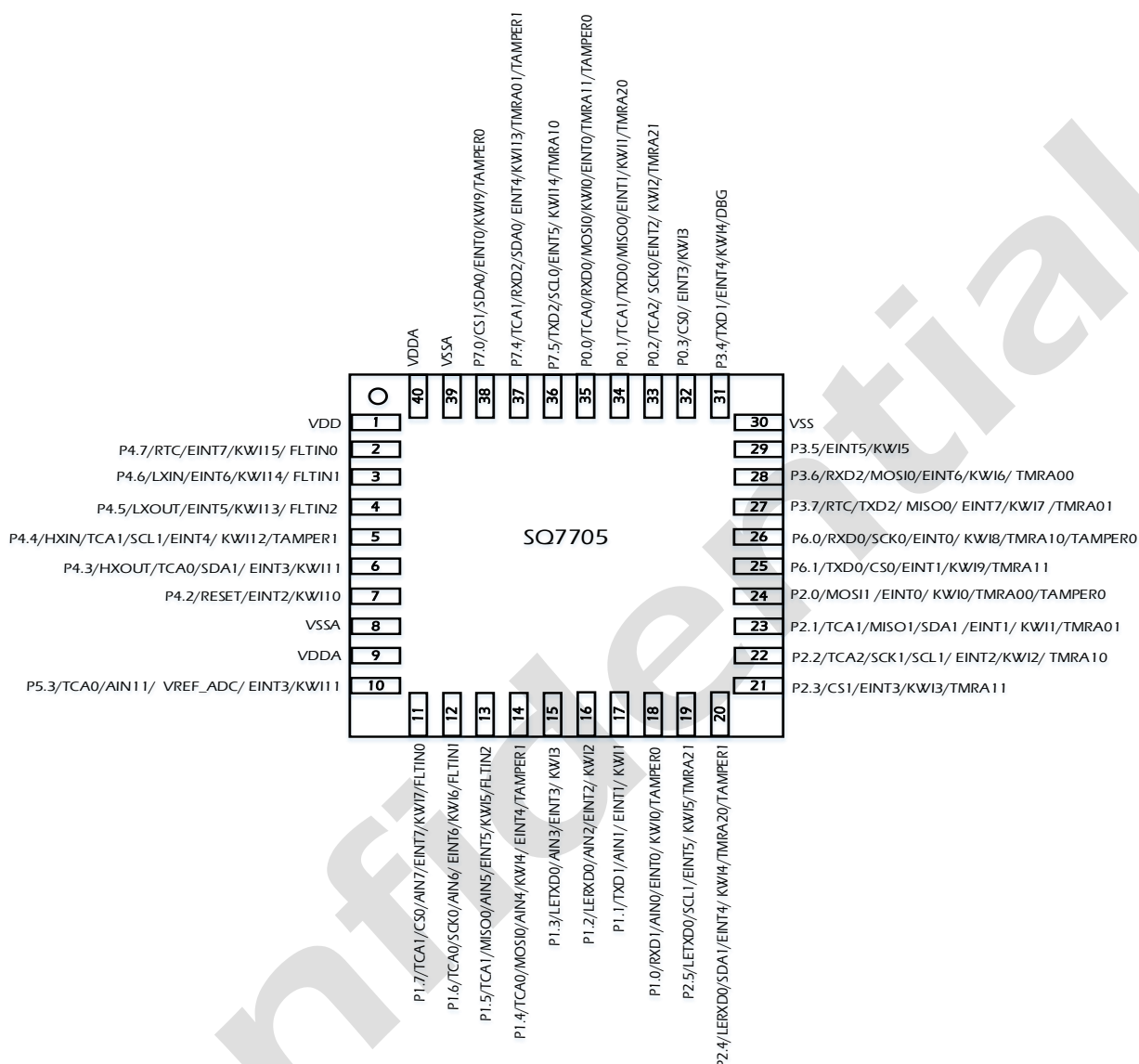
Product No.: SQ7705N5040SGGR (QFN40 5x5)

Figure 2-3 Pin Assignment of SQ7705 (QFN40)

Note 1: SQ7705 simulation needs to connect P3.4/DBG, P4.2/RESET, VDD, and VSS. For the simulation pins reserved by the customer on the system board, please refer to the external reference circuit. It is not recommended to add other components to avoid affecting the simulation characteristics or functions

Note 2: SQ7705 programming is performed by OCDE pins. For the programming pins reserved by the customer on the system board, please refer to the external reference circuit. It is not recommended to add other components to avoid affecting the programming characteristics or Function. 4-wire OCDE pin: Same as the simulation pin (P3.4/DBG, P4.2/RESET, VDD, and VSS). It takes about (7) seconds to burn the 64KByte program space in a single IC. iMQ emulator (MQ-Link) and writer support this burning mode.

No.：TDDS01-S7705-EN(B)	Name：SQ7705 Brief Datasheet	Version：V1.2

64 Pin.	40 Pin	Pin Name/Pin Option	I/O Type	Function Description
1	1	VDD	Power	Positive power supply.
2	2	P4.7/RTC/EINT7/KWI15/ FLTIN0	I/O (Type A)	P4.7 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. RTC, external interrupt EINT7, wake up pin KWI15, 8/16-bit timer FLTIN0 input are pin-shared with P4.7.
3	3	P4.6/LXIN/EINT6/KWI14/ FLTIN1	I/O (Type B)	P4.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. LXIN, external interrupt EINT6, wake up pin KWI14, 8/16-bit timer FLTIN1 input are pin-shared with P4.6. LXIN is connected to low frequency external crystal.
4	4	P4.5/LXOUT/EINT5/KWI13/ FLTIN2	I/O (Type B)	P4.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. LXOUT, external interrupt EINT5, wake up pin KWI13, 8/16-bit timer FLTIN2 input are pin-shared with P4.5. LXOUT is connected to low frequency external crystal.
5	5	P4.4/HXIN/TCA1/SCL1/ EINT4/ KWI12/TAMPER1	I/O (Type B)	P4.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. HXIN, 16-bit timer TCA1, SCL1 (I2C bus clock input/output), external interrupt EINT4, wake up pin KWI12 and TAMPER1 are pin shared with P4.4. HXIN is connect to high frequency external crystal.
6	6	P4.3/HXOUT/TCA0/SDA1/ EINT3/KWI11	I/O (Type B)	P4.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. HXOUT, 16-bit timer TCA0, SDA1 (I2C bus data input/output), external interrupt EINT3, wake up pin KWI11 are pin-shared with P4.3. HXOUT is connected to high frequency external crystal.

7	7	P4.2/RESET/EINT2/KWI10	I/O (Type A)	P4.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. External interrupt EINT2, wake up pin KWI10 are pin-shared with P4.2. RESET is pin-shared with P4.2. Reset is low-active.
8		P5.7/TCA2/CS1/AIN15/ EINT7/KWI15	I/O (Type C)	P5.7 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. 16-bit timer TCA2, CS1 (SPI chip select), ADC input AIN15, external interrupt EINT7, wake up pin KWI15 are pin-shared with P5.7.
9		P5.6/TCA2/SCK1/DVO/ AIN14/EINT6/ KWI14	I/O (Type C)	P5.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistors. 16-bit timer TCA2, SCK1 (SPI clock), divider output (DVO), ADC input AIN14, external interrupt EINT6, wake up pin KWI14 are pin-shared with P5.6.
10		P5.5/MISO1/AIN13/EINT5/ KWI13	I/O (Type C)	P5.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. MISO1 (SPI master in salve out), ADC input AIN13, external interrupt EINT5, wake up pin KWI13 are pin-shared with P5.5.
11		P5.4/MOSI1/AIN12/EINT4/ KWI12/TAMPER1	I/O (Type C)	P5.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. MOSI1 (SPI master out slave in), ADC input AIN12, external interrupt EINT4, wake up pin KWI12 and TAMPER1 are pin-shared with P5.4.
12	8	VSSA	GND	Analog power ground
13	9	VDDA	Power	Analog positive power supply.
14	10	P5.3/TCA0/AIN11/ VREF_ADC/EINT3/KWI11	I/O (Type C)	P5.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, ADC input AIN11, VREF_ADC, external interrupt EINT3, wake up pin KWI11 are pin-shared with P5.3.

15		P5.2/TCA2/AIN10/EINT2/ KWI10	I/O (Type C)	P5.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA2, ADC input AIN10, external interrupt EINT2, wake up pin KWI10 are pin-shared with P5.2.
16		P5.1/TCA1/TXD1/AIN9/ EINT1/KWI9	I/O (Type C)	P5.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, UART TXD1, ADC input AIN9, external interrupt EINT1, wake up pin KWI9 are pin-shared with P5.1.
17		P5.0/TCA0/RXD1/AIN8/ EINT0/KWI8/TAMPER0	I/O (Type C)	P5.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, UART RXD1, ADC input AIN8, external interrupt EINT0, wake up pin KWI8 and TAMPER0 are pin-shared with P5.0.
18		VSS	GND	Ground
19		VDD	Power	Positive power supply.
20	11	P1.7/TCA1/CS0/AIN7/EINT7/KWI7/FLTIN0	I/O (Type C)	P1.7 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, CS0 (SPI chip select), ADC input AIN7, external interrupt EINT7, wake up pin KWI7,8/16-bit timer FLTIN0 input are pin-shared with P1.7.
21	12	P1.6/TCA0/SCK0/AIN6/ EINT6/KWI6/FLTIN1	I/O (Type C)	P1.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, SCK0 (SPI clock input/output), ADC input AIN6, external interrupt EINT6, wake up pin KWI6, 8/16-bit timer FLTIN1 input are pin-shared with P1.6.

22	13	P1.5/TCA1/MISO0/AIN5/ EINT5/KWI5/FLTIN2	I/O (Type C)	P1.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, MISO0 (SPI master in slave out), ADC input AIN5, external interrupt EINT5, wake up pin KWI5, 8/16-bit timer FLTIN2 input are pin-shared with P1.5.
23	14	P1.4/TCA0/MOSI0/AIN4/ KWI4/EINT4/TAMPER1	I/O (Type C)	P1.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, MOSI0 (SPI master out slave in), ADC input AIN4, external interrupt EINT4, wake up pin KWI4 and TAMPER1 are pin-shared with P1.4.
24	15	P1.3/LETXD0/AIN3/EINT3/ KWI3	I/O (Type C)	P1.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LETXD0, ADC input AIN3, external interrupt EINT3, wake up pin KWI3 are pin-shared with P1.3.
25	16	P1.2/LERXD0/AIN2/EINT2/ KWI2	I/O (Type C)	P1.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LERXD0, ADC input AIN2, external interrupt EINT2, wake up pin KWI2 are pin-shared with P1.2.
26	17	P1.1/TXD1/AIN1/ EINT1/ KWI1	I/O (Type C)	P1.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART TXD1, ADC input AIN1, external interrupt EINT1, wake up pin KWI1 are pin-shared with P1.1.
27	18	P1.0/RXD1/AIN0/EINT0/ KWI0/TAMPER0	I/O (Type C)	P1.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART RXD1, ADC input AIN0, external interrupt EINT0, wake up pin KWI0 and TAMPER0 are pin-shared with P1.0.
28		P2.6/TCA2/EINT6/KWI6	I/O (Type C)	P2.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor.

				16-bit timer TCA2, external interrupt EINT6, wake up pin KWI6 are pin-shared with P2.6.
29	19	P2.5/LETXD0/SCL1/EINT5/ KWI5/TMRA21	I/O (Type C)	P2.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LETXD0, SCL1 (I2C clock input/output), external interrupt EINT5, wake up pin KWI5, 8/16-bit timer TMRA21 are pin-shared with P2.5.
30	20	P2.4/LERXD0/SDA1/EINT4/ KWI4/TMRA20/TAMPER1	I/O (Type C)	P2.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LERXD0, SDA1 (I2C data input/output), external interrupt EINT4, wake up pin KWI4, 8/16-bit timer TMRA20 and TAMPER1 are pin-shared with P2.4.
31		VSS	GND	Ground
32		VDD	Power	Positive power supply.
33	21	P2.3/CS1/EINT3/KWI3/ TMRA11	I/O (Type A)	P2.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. CS1 (SPI chip select), external interrupt EINT3, wake up pin KWI3, 8/16-bit timer TMRA11 are pin-shared with P2.3.
34	22	P2.2/TCA2/SCK1/SCL1/ EINT2/KWI2/TMRA10	I/O (Type A)	P2.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA2, SCK1 (SPI clock input/output), SCL1 (I2C clock input/output), external interrupt EINT2, wake up pin KWI2, 8/16-bit timer TMRA10 are pin-shared with P2.2.
35	23	P2.1/TCA1/MISO1/SDA1/ EINT1/ KWI1/TMRA01	I/O (Type A)	P2.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, MISO1 (SPI master in slave out), SDA1 (I2C data input/output), external interrupt

				EINT1, wake up pin KWI1, 8/16-bit timer TMRA01are pin-shared with P2.1.
36	24	P2.0/MOSI1 /EINT0/ KWI0/TMRA00/TAMPER0	I/O (Type A)	P2.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. MOSI1 (SPI master out slave in), external interrupt EINT0, wake up pin KWI0, 8/16-bit timer TMRA00 and TAMPER0 are pin-shared with P2.0.
37		P6.6/TCA1/TXD0/EINT6/KWI14/ FLTIN0	I/O (Type A)	P6.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, UART TXD0, external interrupt EINT6, wake up pin KWI14, 8/16-bit timer FLTIN0 input are pin-shared with P6.6.
38		P6.5/TCA0/RXD0/EINT5/KWI13/FLTIN1	I/O (Type A)	P6.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, UART RXD0, external interrupt EINT5, wake up pin KWI13, 8/16-bit timer FLTIN1 input are pin-shared with P6.5.
39		P6.4/TCA2/EINT4/KWI12/ FLTIN2/TAMPER1	I/O (Type A)	P6.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA2, external interrupt EINT4, wake up pin KWI12, 8/16-bit timer FLTIN2 and TAMPER1 input are pin-shared with P6.4.
40		P6.3/TCA1/TMRA21/EINT3/ KWI11	I/O (Type A)	P6.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, external interrupt EINT3, wake up pin KWI11, 8/16-bit timer TMRA21 are pin-shared with P6.3.
41		P6.2/DVO/EINT2/KWI10/ TMRA20	I/O (Type A)	P6.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Divider output DVO, external interrupt EINT2, wake up pin KWI10, 8/16-bit timer TMRA20 are pin-shared with P6.2.

42	25	P6.1/TXD0/CS0/EINT1/KWI9/TA11	I/O (Type A)	P6.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART TXD0, CS0 (SPI chip select), external interrupt EINT1, wake up pin KWI9 are pin-shared with P6.1.
43	26	P6.0/RXD0/SCK0/EINT0/ KWI8/TA10/TAMPER0	I/O (Type A)	P6.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART RXD0, SCK0 (SPI clock input/output), external interrupt EINT0, wake up pin KWI8, 8/16-bit timer TA10 and TAMPER0 are pin-shared with P6.0.
44	27	P3.7/RTC/TXD2/ MISO0/ EINT7/KWI7/TA01	I/O (Type A)	P3.7 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. RTC, UART TXD2, SPI MISO0, external interrupt EINT7, wake up pin KWI 7, 8/16 timer TA01 are pin-shared with P3.7.
45	28	P3.6/RXD2/MOSI0/EINT6/KWI6/TA00	I/O (Type A)	P3.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART RXD2, SPI MOSI0, external interrupt EINT6, wake up pin KWI6, 8/16 timer TA00 are pin-shared with P3.6.
46	29	P3.5/EINT5/KWI5	I/O (Type A)	P3.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. External interrupt EINT5, wake up pin KWI5 are pin-shared with P3.7.
47	30	VSS	GND	Ground
48		VDD	Power	Positive power supply.
49	31	P3.4/TXD1/EINT4/KWI4/DBG	I/O (Type A)	P3.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART TXD1, external interrupt EINT4, wake up pin KWI4 are pin-shared with P3.4.

50		P0.7/TCA0/RXD1/CS0/EINT7/KWI7	I/O (Type A)	P0.7 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, UART RXD1, CS0 (SPI chip select), external interrupt EINT7, wake up pin KWI7 are pin-shared with P0.7.
51		P0.6/LETXD0/SCK0/ EINT6 /KWI6	I/O (Type A)	P0.6 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LETXD0, SCK0 (SPI clock input/output), external interrupt EINT6, wake up pin KWI6 are pin-shared with P0.6.
52		P0.5/LERXD0/MISO0/EINT5/KWI5/	I/O (Type A)	P0.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. Low energy UART LERXD0, MISO0 (SPI master in slave out), external interrupt EINT5, wake up pin KWI5 are pin-shared with P0.5.
53		P0.4/MOSI0 /EINT4/KWI4/TAMPER1	I/O (Type A)	P0.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. MOSI0 (SPI master out slave in), external interrupt EINT4, wake up pin KWI4 and TAMPER1 are pin-shared with P0.4.
54	32	P0.3/CS0/ EINT3/KWI3	I/O (Type A)	P0.3 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. CS0 (SPI chip select), external interrupt EINT3, wake up pin KWI3 are pin-shared with P0.3.
55	33	P0.2/TCA2/ SCK0/EINT2/ KWI2/TMRA21	I/O (Type A)	P0.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA2, SCK0 (SPI clock input/output), external interrupt EINT2, wake up pin KWI2, 8/16-bit timer TMRA21 are pin-shared with P0.2.
56	34	P0.1/TCA1/TXD0/MISO0/EINT1/KWI1/TMRA20	I/O (Type A)	P0.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, UART TXD0, MISO0 (SPI master in slave out), external interrupt EINT1, wake up pin

|				KWI1, 8/16-bit timer TMRA20 are pin-shared with P0.1.
57	35	P0.0/TCA0/RXD0/ MOSI0/ EINT0/KWI0 /TMRA11/TAMPER0	I/O (Type A)	P0.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA0, UART RXD0, MOSI0 (SPI master out slave in), external interrupt EINT0, wake up pin KWI0, 8/16-bit timer TMRA11 and TAMPER0 are pin-shared with P0.0.
58	36	P7.5/TXD2/SCL0/EINT5/ KWI14/TMRA10	I/O (Type A)	P7.5 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. UART TXD2, SCL0 (I2C clock input/output), external interrupt EINT5, wake up pin KWI14,8/16-bit timer TMRA10 are pin-shared with P7.5.
59	37	P7.4/TCA1/RXD2/SDA0/ EINT4/KWI13/TMRA01 TAMPER1	I/O (Type A)	P7.4 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. 16-bit timer TCA1, UART RXD2, SDA0 (I2C data input/output), external interrupt EINT4, wake up pin KWI 13, 8/16-bit timer TMRA01 and TAMPER1 are pin-shared with P7.4.
60		P7.2/EINT2/KWI11/TMRA00	I/O (Type A)	P7.2 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. External interrupt EINT2, wake up pin KWI11,8/16-bit timer TMRA00 are pin-shared with P0.1.
61		P7.1/SCL0/EINT1/KWI9	I/O (Type A)	P7.1 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. SCL0 (I2C clock input/output), external interrupt EINT1, wake up pin KWI9 are pin-shared with P7.1.
62	38	P7.0/CS1/SDA0/EINT0/KWI8 TAMPER0	I/O (Type A)	P7.0 is bi-directional I/O pins, which are software configurable to be with pull-up or pull-down resistor. CS1 (SPI chip select), SDA0 (I2C data input/output), external interrupt EINT0, wake up pin KWI8 and TAMPER0 are pin-shared with P7.0.

63	39	VSSA		GND	Analog power ground
64	40	VDDA		Power	Analog positive power supply.

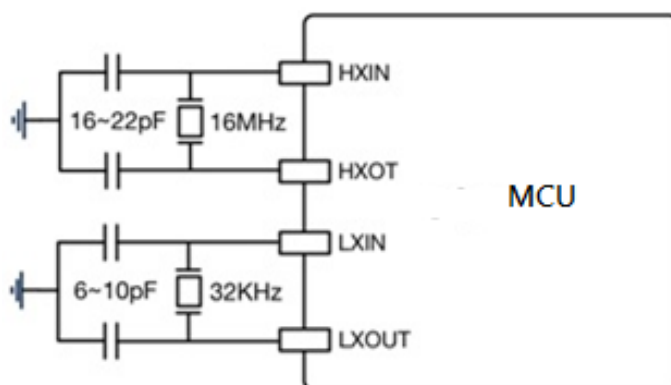Recommended external application circuits as below figures, please follow the recommendation to design:
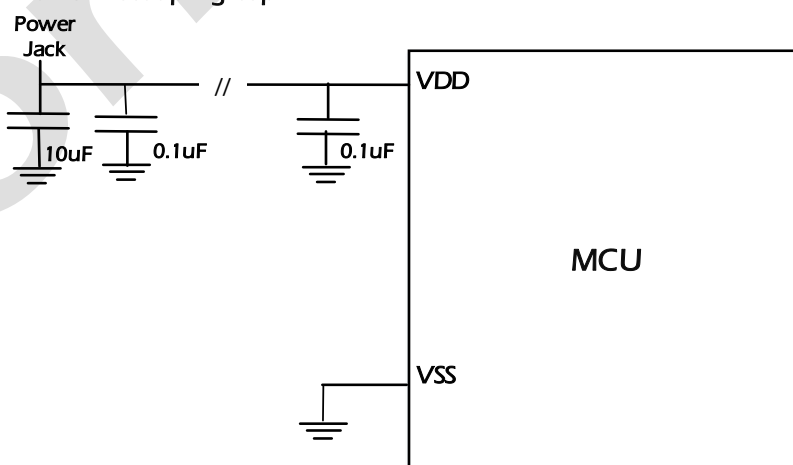
1. **ADC Input Filter :**

ADC Input Filter
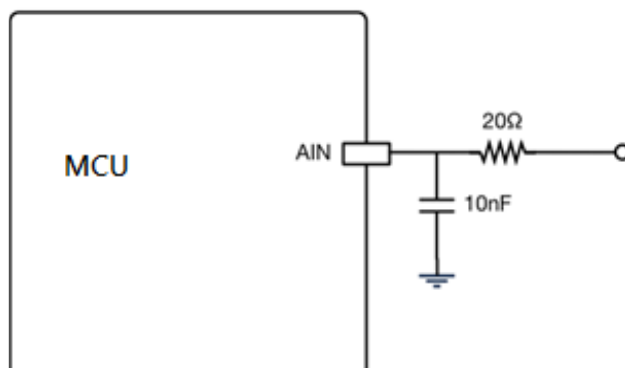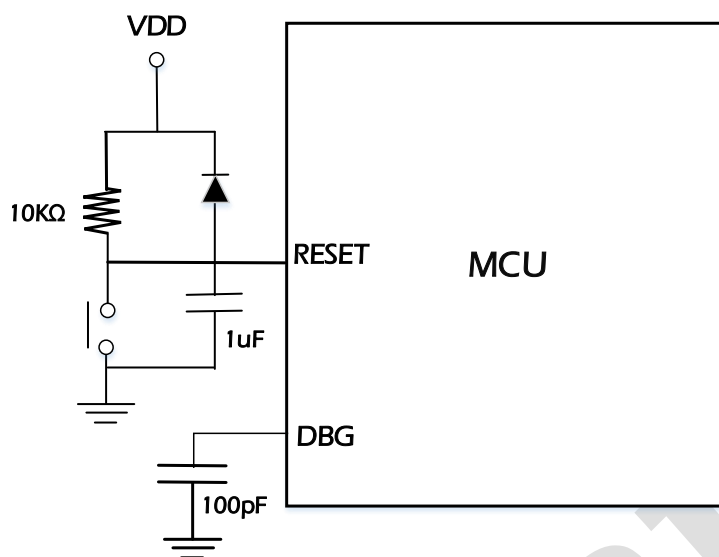

2. **External Crystal :**

External Crystal

3. **Power decoupling :**
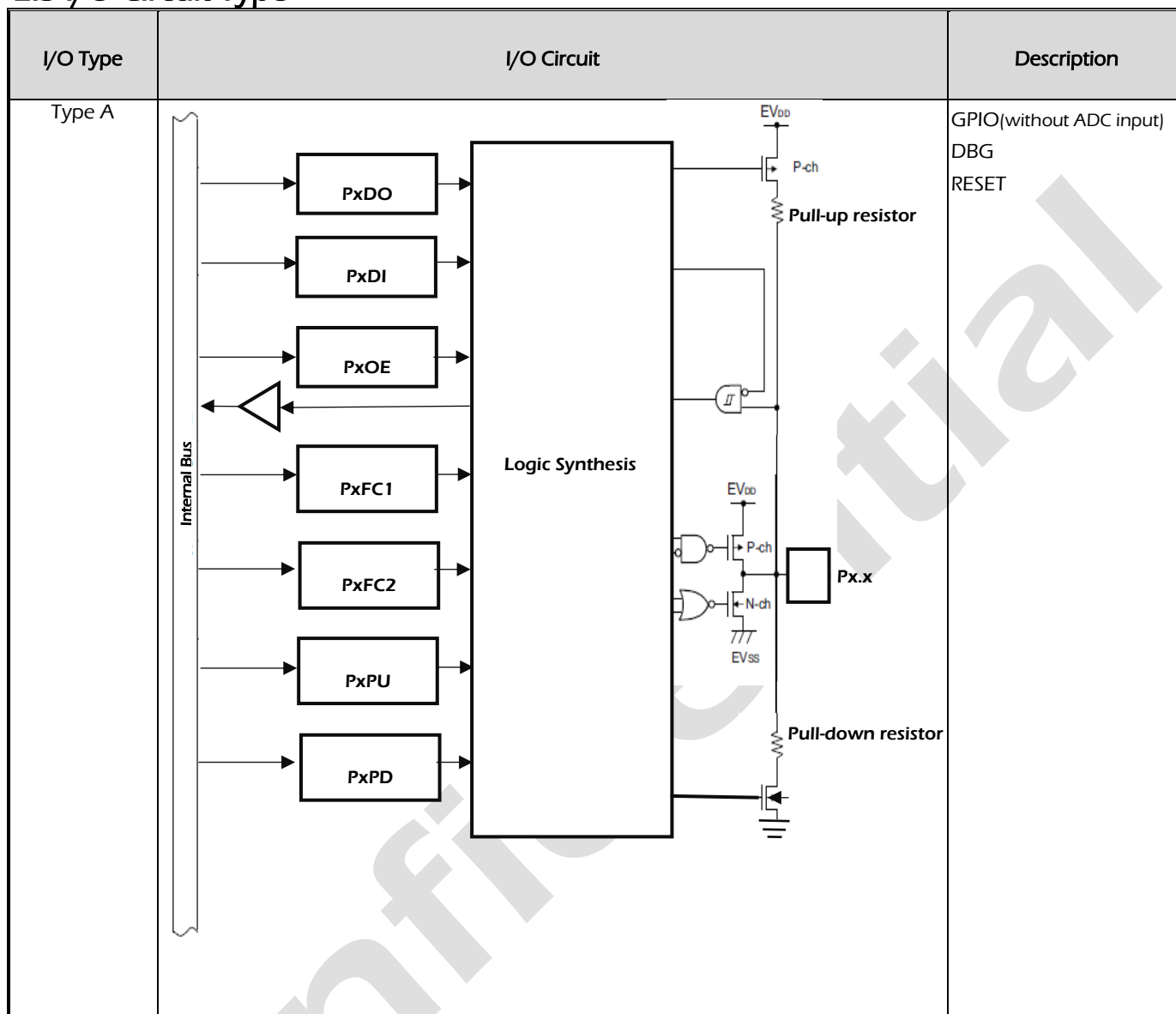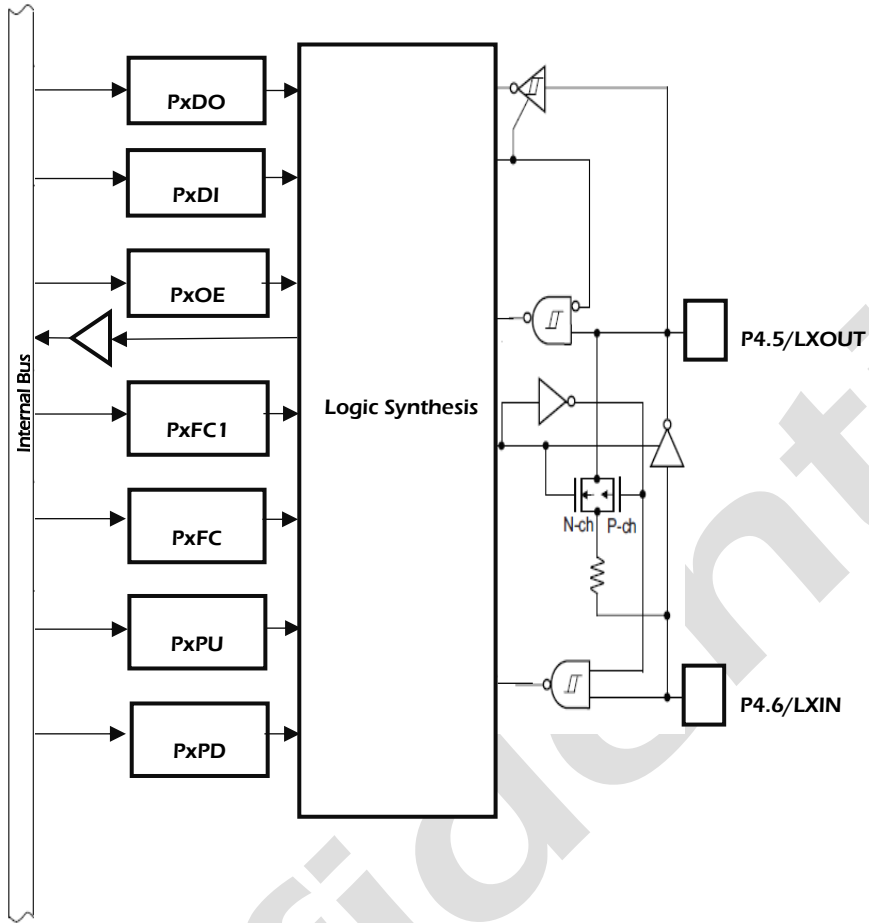
Power Decoupling Cap

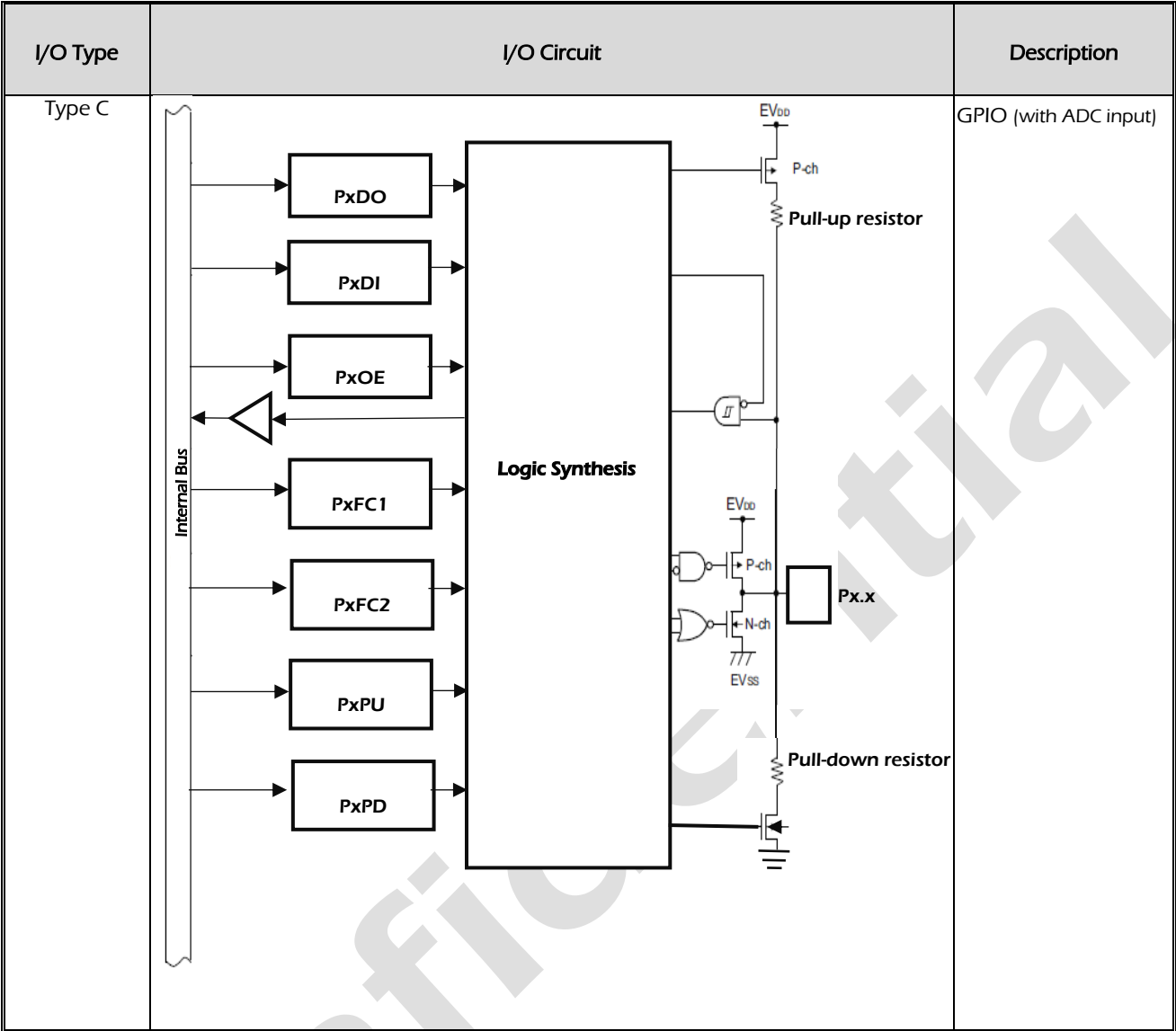Note：The 0.1uF near the VDD should be as close as possible to the IC

4. <u>RESET and DBG pin :</u>

2.3 I/O Circuit Type

I/O Type	I/O Circuit	Description
Type A		GPIO(without ADC input) DBG RESET

I/O Type	I/O Circuit	Description
Type B		Connect to external crystal

I/O Type	I/O Circuit	Description
Type C		GPIO (with ADC input)

3. Electrical Characteristics

3.1 Absolute Maximum Rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

$(V_{SS} = 0V)$

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}	–	-0.3 to 6.0	V
Input Voltage	V_{IN}	All I/O pins	-0.3 to VDD+0.3	V
Output Current(total)	I_{OUT}	All I/O pins	100	mA
Storage Temperature	T_{STG}	–	-50 to 125	℃

3.2 Operation Conditions

The following defines the electrical characteristics of the device when it is operated at voltage and temperature maximum/minimum values. Unless otherwise stated, the standard conditions were determined at "operating temperature 25 ° C and operating voltage VDD = 5 V."

3.2.1 Operation Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	2.0	3.3	5.5	V
Analog Supply Voltage	V_{DDA}	2.0	3.3	5.5	V
Reset Voltage (Note)	V_{RST}	1.85	1.90	1.95	V
Operating Temperature	Ta	-40	25	85	°C

Note: Reset voltage uses BROR

3.2.2 Clock Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External Clock Source						
Low Frequency External Crystal	f_{LXIN}	--	--	32768	--	Hz
High Frequency External Crystal	f_{XIN}	--	1	--	16	MHz
Internal Clock Source						
High Frequency Internal Oscillator (PLL)[Note1]	f_{PLL}	$T_A = 25°C$	- 1%	48	+ 1%	MHz
		$T_A = 0~ 50°C$ [Note 2]	- 1%	48	+ 1%	
		$T_A = -20~ 70°C$ [Note 2]	- 1.5%	48	+ 1.5%	
		$T_A = -40~ 85°C$	- 2%	48	+ 2%	
Low Frequency Internal Oscillator	f_{LIRC}	$T_A = 25°C$	-15%	32	+ 15%	kHz
		$T_A = -40~ 85°C$	-30%	32	+ 30%	

Note 1：High frequency external crystal(HXIN) can be PLL clock source. When high frequency external crystal (HXIN) is PLL clock source, the external crystal (HXIN) must be 8MHz.

Note 2：The spec is under VDD= 5V ±10% (4.5~5.5V) condition.

3.2.3 I/O Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}	-	0	-	0.25 VDD	V
Input high voltage	V_{IH}	-	0.75 VDD	-	VDD	V
Output low voltage	V_{OL1}	P0DSEL=0, IOL=2.5mA, VDD=3.3V	-	-	0.4	V
	V_{OL2}	P0DSEL=1, IOL=5mA, VDD=3.3V	-	-	0.4	V
Output high voltage	V_{OH1}	P0DSEL=0, IOH=0.75mA, VDD=3.3V	VDD-0.6	-	-	V
	V_{OH2}	P0DSEL=1, IOH=1.5mA, VDD=3.3V	VDD-0.6	-	-	V
Output low current	I_{OL1}	P0DSEL=0, Vo=0.1*VDD, VDD=3.3V	2.5	6.7		mA
		P0DSEL=0, Vo=0.3*VDD, VDD=3.3V	7	15		mA
	I_{OL2}	P0DSEL=1, Vo=0.1*VDD, VDD=3.3V	5	13.4		mA
		P0DSEL=1, Vo=0.3*VDD, VDD=3.3V	14	30		mA
Output high current	I_{OH1}	P0DSEL=0, Vo=0.9*VDD, VDD=3.3V	1	2.4		mA
		P0DSEL=0, Vo=0.7*VDD, VDD=3.3V	3	5.8		mA
	I_{OH2}	P0DSEL=1, Vo=0.9*VDD, VDD=3.3V	2	4.8	-	mA
		P0DSEL=1, Vo=0.7*VDD, VDD=3.3V	6	11.6		mA
Pull-up resistance	R_{PULLUP}	connect to pull-up resistance	10	20	40	kΩ
Pull-low Resistance	R_{PULLDN}	connect to pull-down resistance	10	20	40	kΩ

Note 1: Set P0DSEL to select the pin driving force.

No.：TDDS01-S7705-EN(B)	Name：SQ7705 Brief Datasheet	Version：V1.2

3.3 D.C. Characteristics

			Operating @ 3.3 V，Ta= -40~85℃			
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Normal Mode (Code executing from Flash)	I_{DD_N0}	System clock is PLL(clock source is high frequency internal oscillator) fsysclk= PLL 48MHz	–	8.2	–	mA
	I_{DD_N1}	System clock is HXTAL fsysclk= HXTAL16MHz	–	4.1	–	mA
	I_{DD_N2}	System clock is LIRC fsysclk= LIRC 32KHz	–	1.2	–	mA
	I_{DD_N3}	System clock is LXTAL fsysclk= LXTAL 32768Hz	–	1.2	–	mA
Sleep Mode (CPU clock is stopped)	I_{DD_SL0}	System clock is PLL(clock source is high frequency internal oscillator) fsysclk= PLL 48MHz	–	4.6	–	mA
	I_{DD_SL1}	System clock is HXTAL fsysclk= HXTAL16MHz	–	2.5	–	mA
	I_{DD_SL2}	System clock is LIRC fsysclk= LIRC 32KHz	–	1.2	–	mA
	I_{DD_SL3}	System clock is LXTAL fsysclk= LXTAL 32768Hz	–	1.2	–	mA
Deep Sleep Mode (CPU and RAM are retained)	I_{DD_DS0}	RTC Disable	–	0.6	–	uA
	I_{DD_DS1}	RTC Enable , LXTAL On	–	0.6	–	uA

3.4 Power-on Reset Characteristics

					Vss=0，Ta=-40~85℃	
Symbol	Condition	Min.	Typ.	Max.	Unit
tPPW	Power-on reset minimum pulse width	1	-	-	ms
tPWUP	Warming-up time after a reset is clear and CPU ready	-	4	-	ms
tVDD	Power supply rise time	0.5		5	ms

Note: tPWUP does not include BOOTROM code execution time.
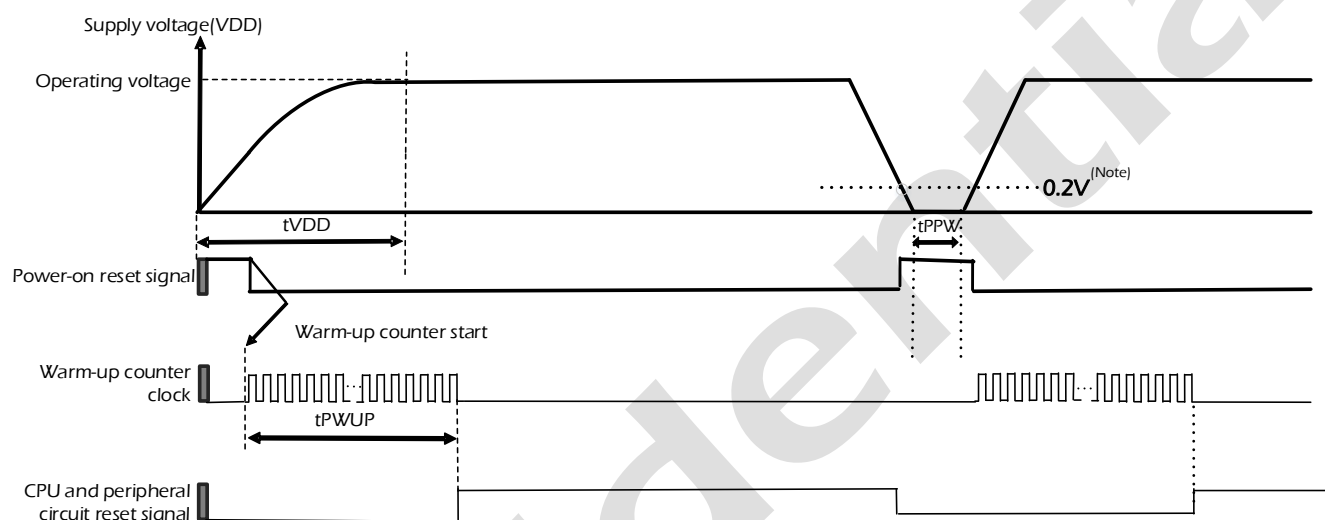
Figure 3-1 Operation Timing of Power-on Reset

Note：In power-down process, the VDD must be 0.2V, then re-power-on to ensure the IC operating normal.

3.5 BROR Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BROR detected voltage	VBROR_Rising	VDD rise time and fall time > tVDD (tVDD please refer to ch3.4 POR characteristics)	1.95	2.0	2.05	V
	VBROR_ Falling		1.85	1.90	1.95	V

Symbol	Description	Min.	Typ.	Max.	Unit
tBRTOFF	BROR voltage detection releasing response time	-	1	10	us
tBRTON	BROR voltage detecting detection response time	-	1	10	us
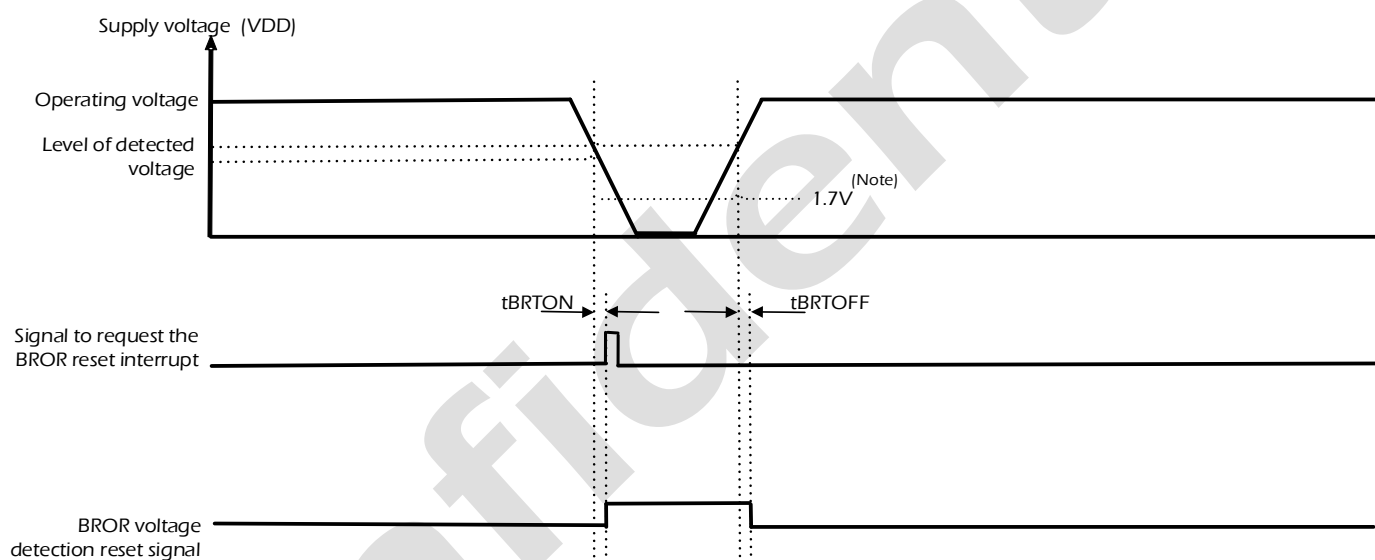
Figure 3-2 BROR

Note：Do not perform any operation when VDD under V1.7V. It will cause the operation abnormal.

3.6 LVD Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LVD0	VD0LVL1	Falling Mode，LVDCR0<LVDCFG>=000 (Note)	1.90	2.00	2.10	V
	VD0LVL2	Falling Mode，LVDCR0<LVDCFG >=001	2.23	2.35	2.47	V
	VD0LVL3	Falling Mode，LVDCR0<LVDCFG >=010	2.52	2.65	2.78	V
	VD0LVL4	Falling Mode，LVDCR0<LVDCFG >=011	2.71	2.85	2.99	V
LVD1	VD1LVL1	Falling Mode，LVDCR1<LVDCFG>=100	2.99	3.15	3.31	V
	VD1LVL2	Falling Mode，LVDCR1<LVDCFG>=101	3.78	3.98	4.18	V
	VD1LVL3	Falling Mode，LVDCR1<LVDCFG>=110	3.99	4.20	4.41	V
	VD1LVL4	Falling Mode，LVDCR1<LVDCFG>=111	4.28	4.50	4.73	V

Symbol	Description	Min.	Typ.	Max.	Unit
tVLTON	Voltage detecting detection response time	-	1	10	us

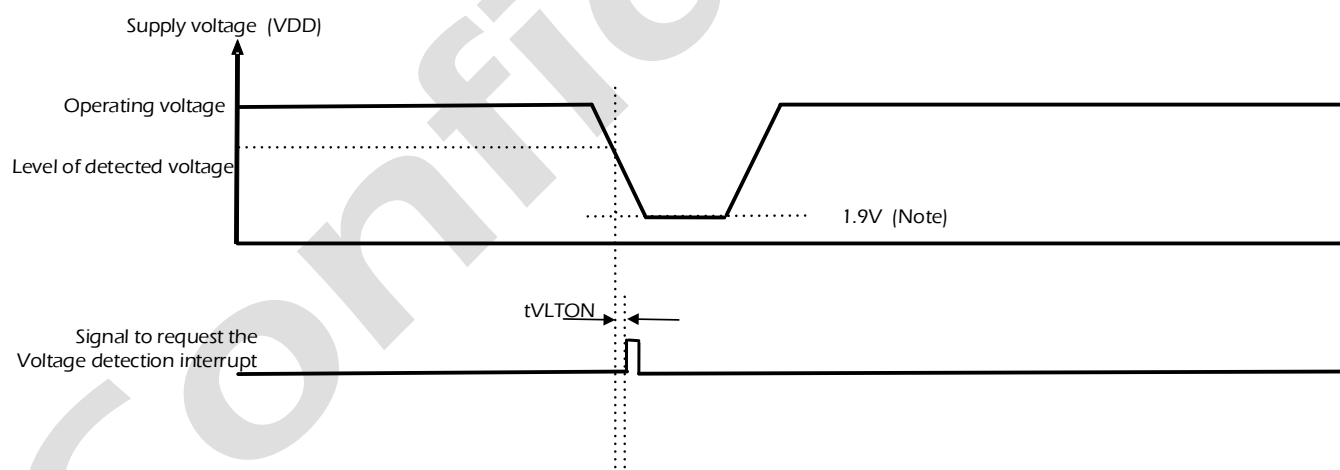

Figure 3- 3 LVD Interrupt

Note: When LVD0 is set to VD0LVL1, BROR may be triggered first when the voltage drops.

3.7 ADC Characteristics

| | | | | VREF_ADC=VDD | |
| | | | | 4.5V $\leq$ VDD $\leq$ 5.5V， T_A= -40~85℃ | |
Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES_{ADC}	–	12	–	bits
Sampling Rate	f_{ADC}	–	–	470	KSPS
Differential Nonlinearity Error (DNL)	DNL_{ADC}	–	–	±2.5	LSB
Integral Nonlinearity Error (INL)	INL_{ADC}	–	–	±3.5	LSB
Gain Error	E_{GAIN}	–	–	±5	LSB
Offset Error	E_{OFFSET}	–	–	±4.5	LSB
Input Voltage Range	V_{ADC_RNG}	–	–	VDD	V
VREF_ADC Voltage Range	V_{REF_ADC}	VDD[Note1]			V
Note 1：VERF_ADC=VDD, the voltage range 4.5~5.5V					
Note 2：Does not include offset and gain compensation					
Note 3：ADC sample rate $= = \frac{1}{22}$ x $\frac{fsysclk}{ADCCKDIV}$					
Example: *When system clock is* 24MHz， ADCCKDIV *set to* 0x02， ADC Sample rate： $\frac{1}{22} x \frac{24\text{MHz}}{2^2} = 272.727$ksps					

| | | | | VREF_ADC=VDD | |
| | | | | 2V $\leq$ VDD < 4.5V， T_A= -40~85℃ | |
Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES_{ADC}	–	12	--	bits
Sampling Rate	f_{ADC}	–	–	470	KSPS
Differential Nonlinearity Error (DNL)	DNL_{ADC}	–	–	±4	LSB
Integral Nonlinearity Error (INL)	INL_{ADC}	–	–	±5	LSB
Gain Error	E_{GAIN}	–	–	±6	LSB
Offset Error	E_{OFFSET}	–	–	±6	LSB
Input Voltage Range	V_{ADC_RNG}	–	–	VDD	V
VREF_ADC Voltage Range	V_{REF_ADC}	VDD[注1]			V
Note 1：VERF_ADC=VDD, the voltage range 2~5.5V					
Note 2：Does not include offset and gain compensation					
Note 3：ADC sample rate $= = \frac{1}{22}$ x $\frac{fsysclk}{ADCCKDIV}$					
Example: *When system clock is* 24MHz， ADCCKDIV set to 0x02， ADC Sample rate： $\frac{1}{22} x \frac{24\text{MHz}}{2^2} = 272.727$ksps					

3.8 Flash Characteristics

$(V_{SS} = 0V, 2.0V \leqq V_{DD} \leqq 5.5V, T_{OPR} = -40\ to\ 85°C)$

Parameter	Condition	Min.	Typ.	Max.	Unit
Number of guaranteed writes to flash memory		–	–	100,000	times
Flash memory write time	Write Time (per byte)	–	–	40	μs
Flash memory erase time	Chip Erase	–	–	40	ms
	Sector Erase (1 sector = 512 bytes)	–	–	5	

3.9 EEPROM Characteristics

$(V_{SS} = 0V，2.0V \leqq V_{DD} \leqq 5.5V，T_{OPR} = -40\ to\ 85°C)$

Parameter	Condition	Min.	Typ.	Max.	Unit
Number of guaranteed writes to EEPROM		–	–	100,000	times
EEPROM write time	Write Time (per byte)	–	–	40	μs
EEPROM erase time	Chip Erase	–	–	40	ms
	Sector Erase (1 sector =32 bytes)	–	–	5	

Appendix A. Product Number Information

Example:

| | SQ | 77 | 05 | LA | 064 | S | G | G | R |

iMQ SQ product

Product Series

Sub Series

Package Type

Code	Package	Code	Package
ST	SOT23	SD	SDIP
SP	SOP	LQ	LQFP 7x7
MS	MSOP	LA	LQFP 10x10
SS	SSOP	LE	LQFP 14x14
DP	PDIP	N4	QFN 4x4
TS	TSOP	N5	QFN 5x5
DS	TSSOP		

Pin Count

Code	Package	Code	Package
005	5	032	32
006	6	036	36
008	8	040	40
010	10	044	44
014	14	048	48
016	16	064	64
020	20	080	80
024	24	096	96
028	28	100	100

Program Flash

Data Flash

RAM

Code	Program Flash /Data Flash RAM Size	Code	Program Flash /Data Flash RAM Size
A	128 Bytes	H	16K Bytes
B	256 Bytes	K	24K Bytes
E	512 Bytes	M	32K Bytes
J	1K Bytes	N	40K Bytes
L	2K Bytes	P	48K Bytes
T	4K Bytes	S	64K Bytes
G	8K Bytes	U	96K Bytes
C	12K Bytes	W	128K Bytes

Operating Temp.

Code	Operating Temp.
R	-40~85°C

Appendix B. Package Information

LQFP64 (10x10)
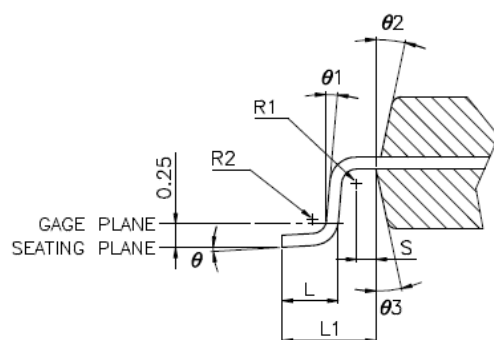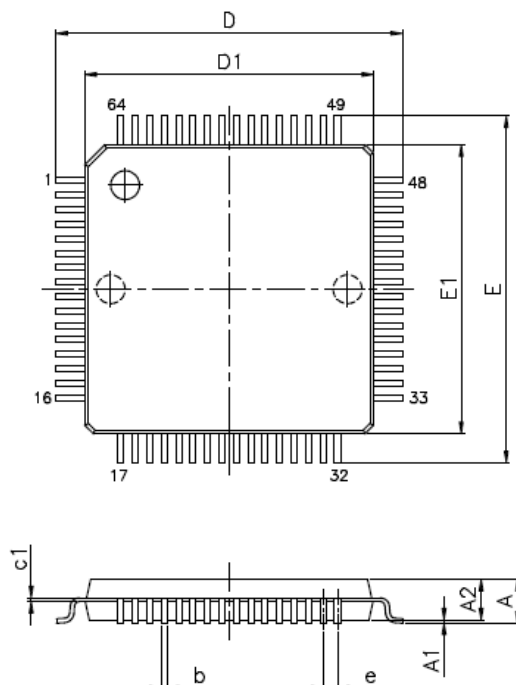
Symbol	mm		
	Min.	Typ.	Max.
A	1.45	1.55	1.65
A1	0.05	–	0.15
A2	1.3	1.4	1.5
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	–	0.75
L1	1.0 REF		

QFN 40(5x5)
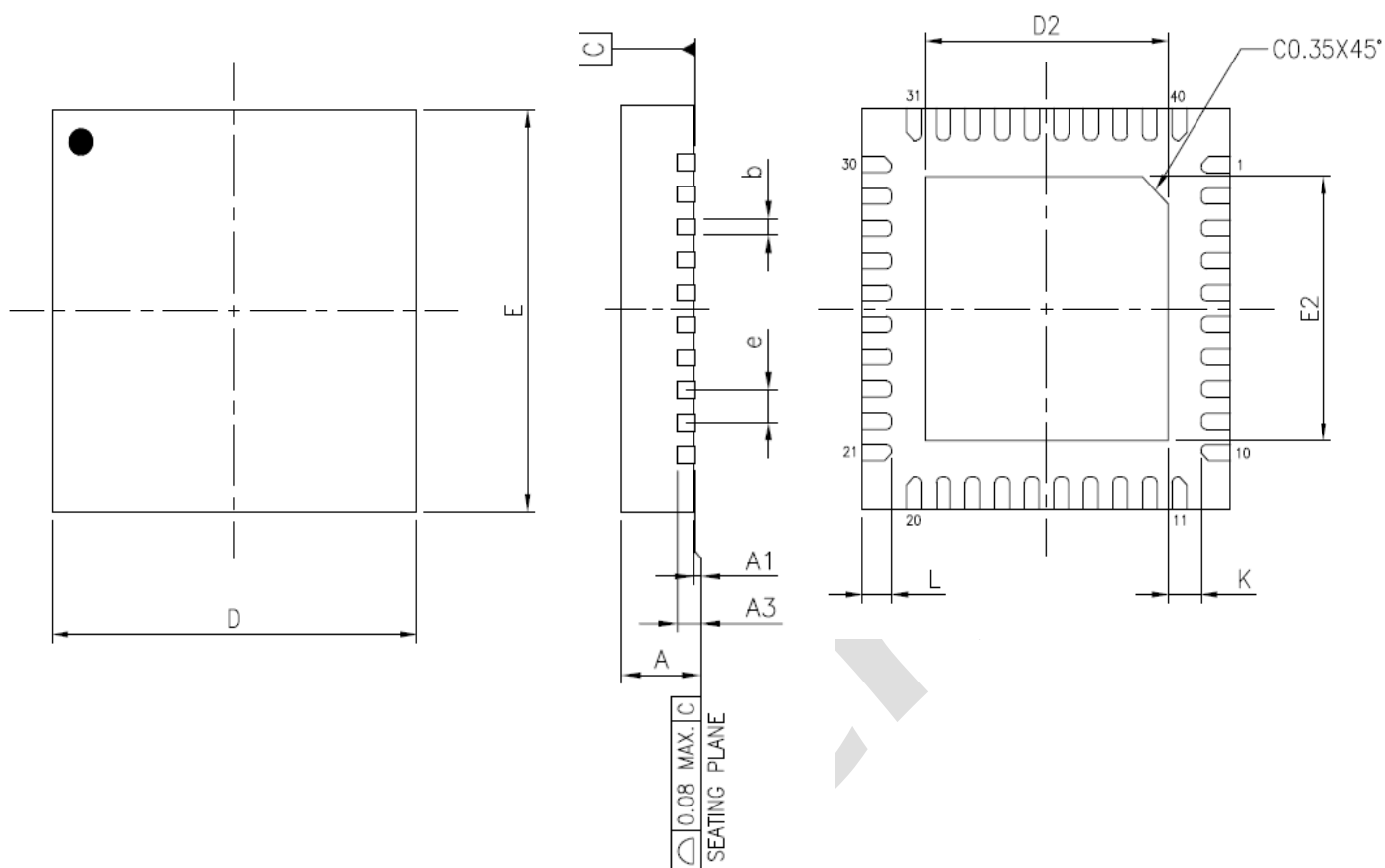
Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.40 BSC		
K	0.20	--	--
D2	3.25	3.30	3.35
E2	3.25	3.30	3.35
L	0.35	0.40	0.45

Appendix C. iMQ IDE Supports ADM Mode and User Mode

i. Establishment and resource planning of ADM project

When creating a new project in iMQ IDE, select "SQ7705.ADM–064—" to create an ADM project.
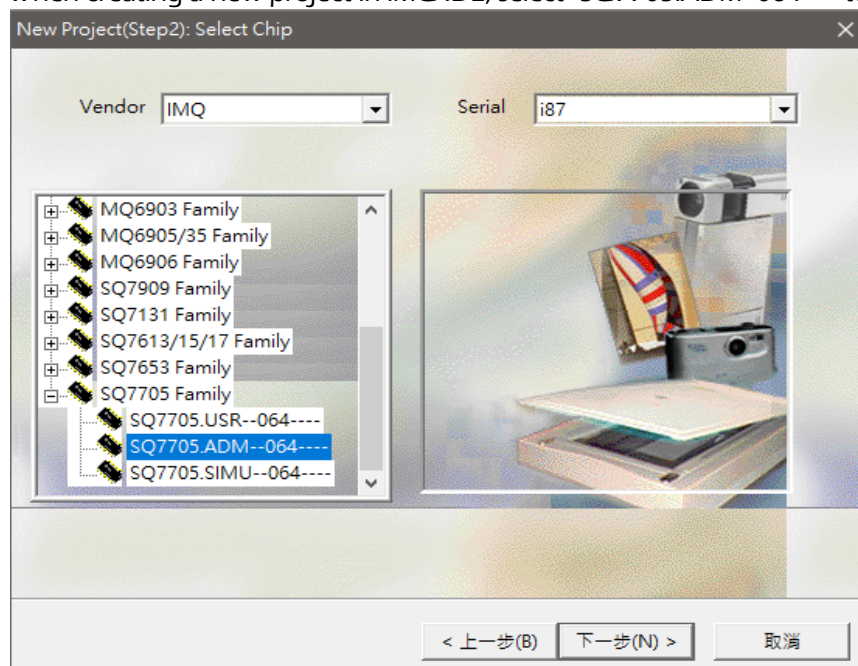
When a new ADM project is created, the "SQ7705 Admin Configuration" window will pop up for resource planning:
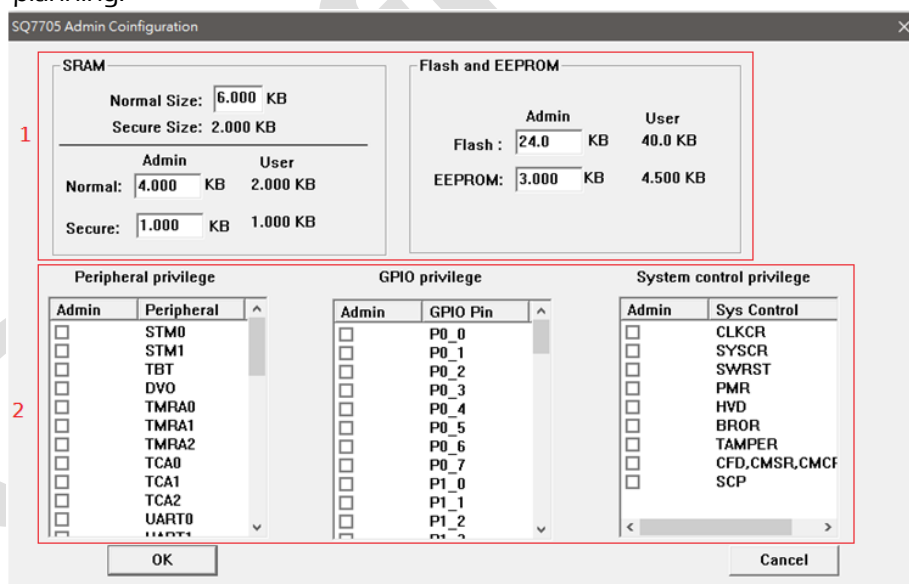
In this window, the followings can be planned.

1. The size of the SRAM, FLASH and EEPROM areas used by ADM and USER modes.

2. Specify whether each peripheral, GPIO, and system control register operate in ADM only or

ADM/USER mode.

3. After pressing "OK," all settings will be saved as a .privCfg file. This file will be used by the ADM project itself and also by the USER mode project.

4. ADM projects and USER projects exist in pairs, and the two communicate and coordinate the use of resources through the .privCfg file.

If the processor is to be operated in ADM mode only, all SRAM, EEPROM and FLASH should be allocated to ADM, and all peripheral devices, GPIO and system control registers should be set to ADM Only.

ii.　USER Project Creation and Resource Viewing

When creating a new project in iMQ IDE, select "SQ7705.USR–064—" to create a USER project.
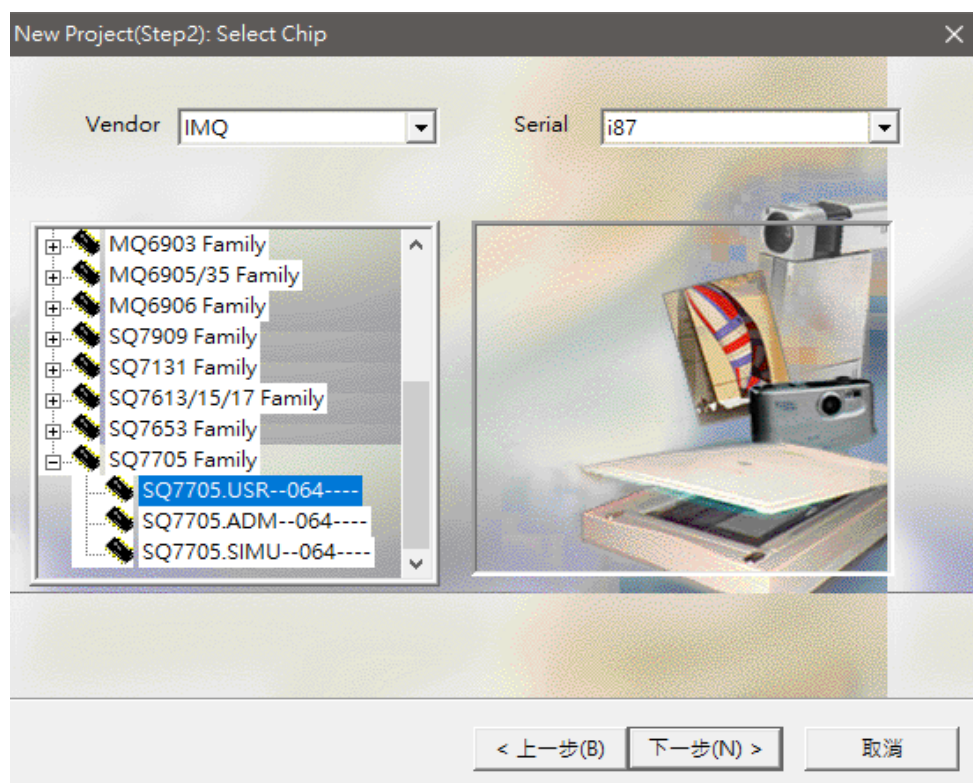

Resources can't be planned or changed in the USER project, but resources allocated to the USER mode can be viewed.

When creating a new project, the requirement for selecting a .privCfg file will pop up. At this place it is necessary to specify the .privCfg file in the corresponding ADM project (to achieve consistency in resource usage between the ADM and USER projects).
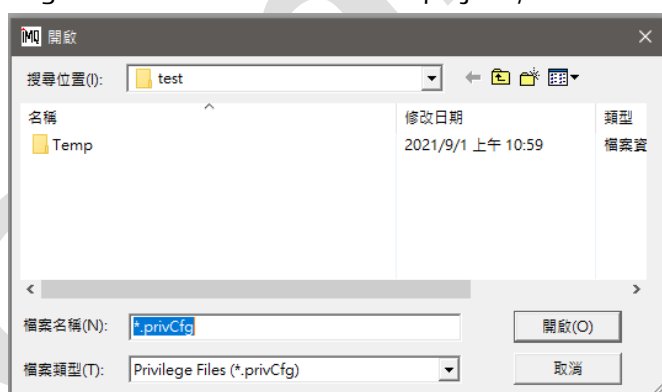
Only resources that can be used in USER mode will appear in the list of peripherals, GPIO, and system control, as shown in the following figure:
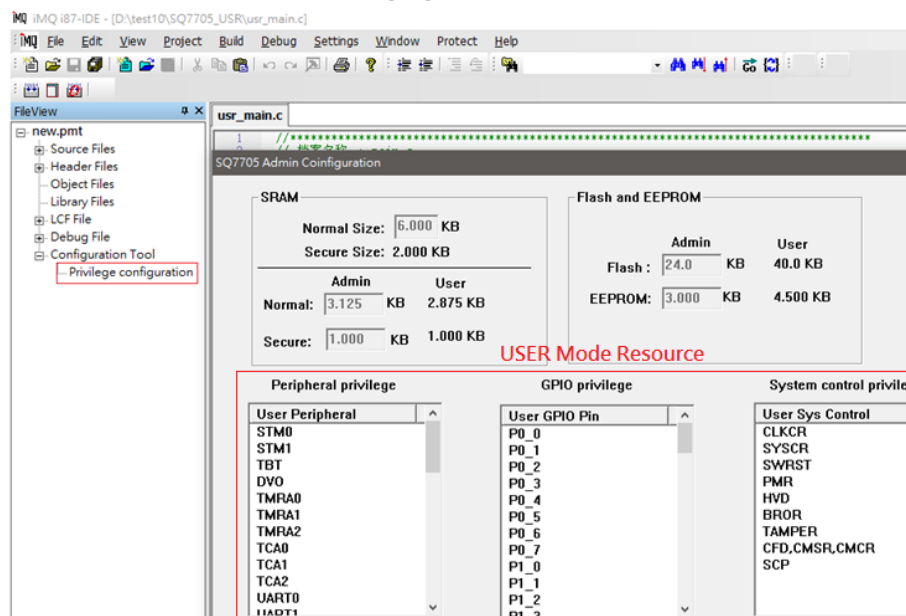

Whenever the ADM project changes the resource file, the USER project also needs to re-import the new resource file.

To re-select the resource file, double-click "Privilege configuration" in FileView to pop up the resource window, then select "Import CFG File" to import the new resource file.
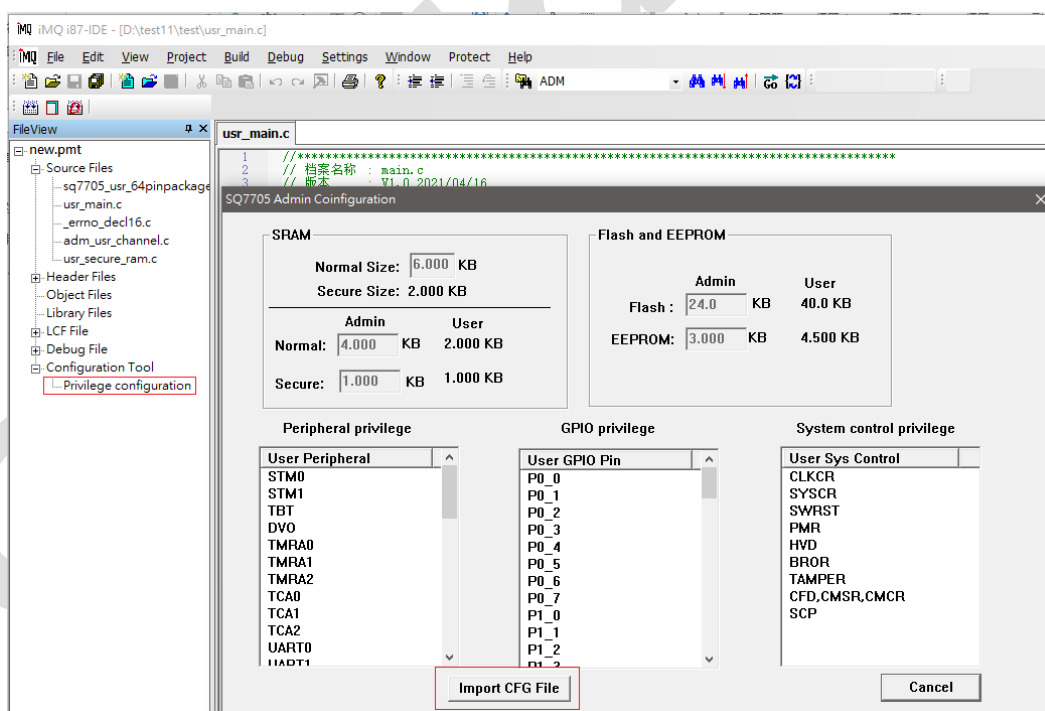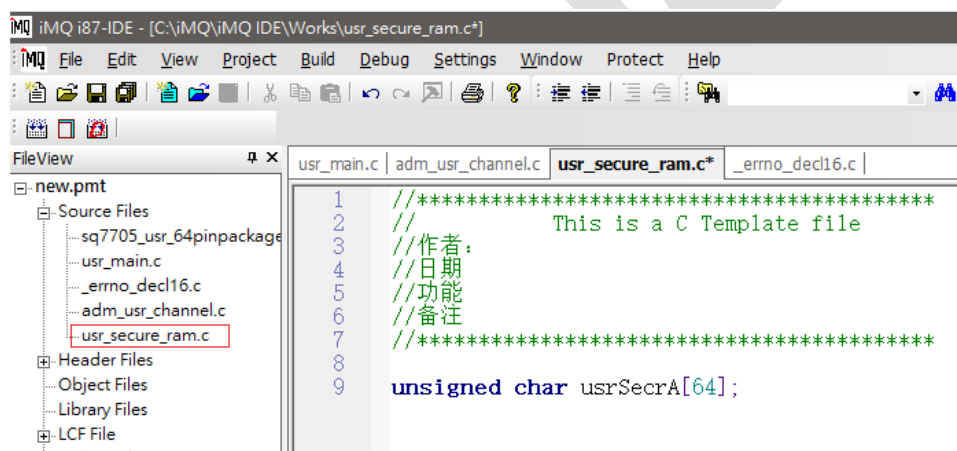
iii. ADM MODE SECURE SRAM

Overall variables declared in adm_secure_ram.c are automatically allocated in the Secure SRAM address area under ADM mode.
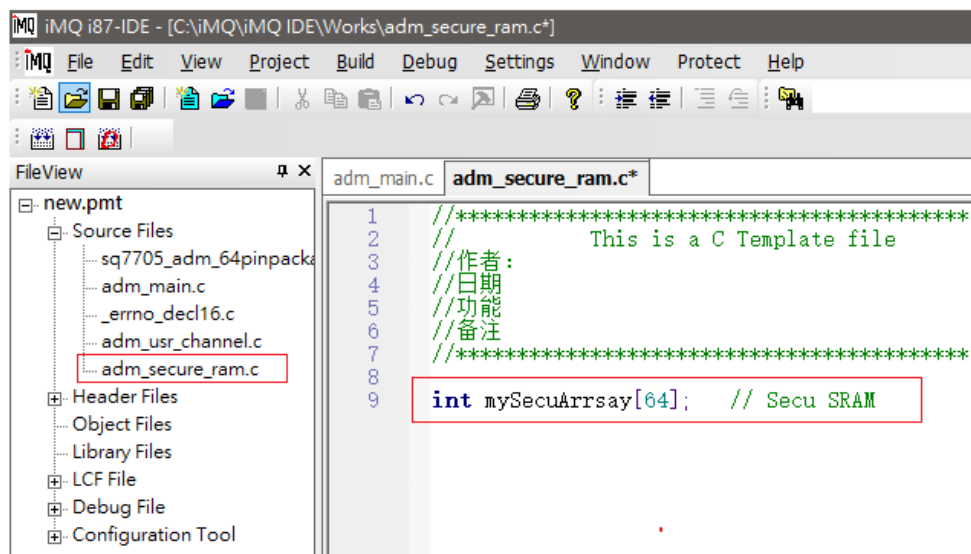
iv. USER MODE SECURE SRAM

Overall variables declared in usr_secure_ram.c will be automatically allocated in the Secure SRAM address area under USER mode.

v. ADM and USER Mode Share SRAM

Data exchange between ADM and USER modes is achieved through Share SRAM memory (this Share SRAM is located in the USER SRAM address space). There is an adm_usr_channel.c file in both ADM and USER projects. The overall variables declared here are the shared memory.

When USER switches to ADM mode, this shared memory can be used to send commands and parameters to ADM mode, and the results of ADM mode operations can also be sent back to USER mode through this shared memory.
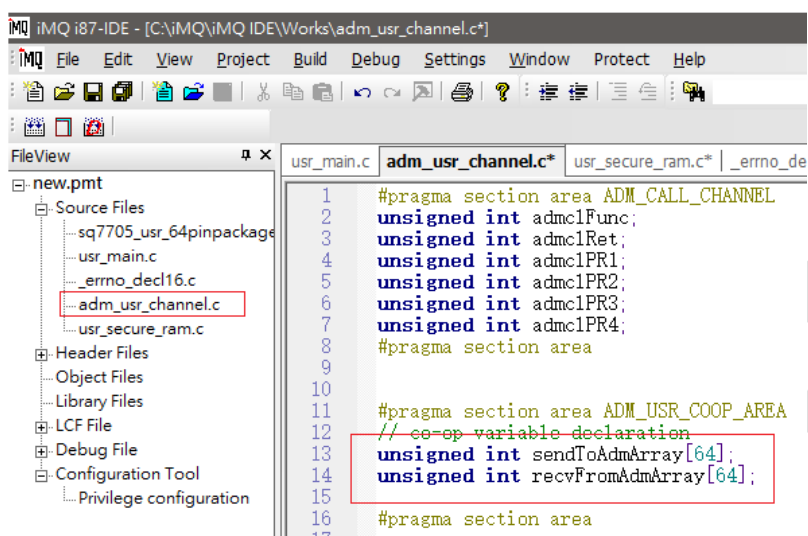
Shared SRAM memory focuses on memory addresses (address areas), not variable names. Thus, these SRAM addresses (address areas) can be handled arbitrarily in ADM and USER projects. They can be declared as different variable names or different structure variables as long as they can access the specified SRSAM memory address.

vi.   USER and ADM Mode Switch

To perform USER-ADM mode switching, both modes follow a fixed procedure.

ADM Mode:

ADM mode uses interrupts to receive mode switching requests from USER, so the ADM U2A interrupt service needs to be started, which can be achieved by setting IFR0 and IER0 bit7.

```
//=========================
//         IFR0
//=========================
#define     IFR0              _0x01A0.byte
#define     IFR_U2A           _0x01A0.bit.b7
#define     IFR_HVD           _0x01A0.bit.b6
#define     IFR_CFD           _0x01A0.bit.b5
#define     IFR_TAMPER        _0x01A0.bit.b4
#define     IFR_WDT           _0x01A0.bit.b3

//=========================
//         IER0
//=========================
#define     IER0              _0x01B0.byte
#define     IER_U2A           _0x01B0.bit.b7
#define     IER_HVD           _0x01B0.bit.b6
#define     IER_CFD           _0x01B0.bit.b5
#define     IER_TAMPER        _0x01B0.bit.b4
```

```
void ADM_main()
{
    // Enable User To Adm IRQ
    __ASM("DI");
    IFR_U2A = 0;
    IER_U2A = 1;
    __ASM("EI");

    // Jump to User mode
    __ASM("NOP");
    __ASM("NOP");
    __ASM("NOP");
    MODEEXC = 0x00;
    while(1);
```

Next, it is necessary to define and enable the ADM U2A interrupt service function, as shown in the following program snippet:

```
void __interrupt U2A_IRQ(void)
{
    // Put cod in here

    // Output result
    MyOutArray[0] = 0x15;

    // GoBack to User Code
    __ASM("NOP");
    __ASM("NOP");
    __ASM("NOP");
    MODEEXC = 0x00;
    __ASM("NOP");
}
```

```
/*                    SQ7705 Interrupt Vector Table Definition
//   [Define interrupt vector table] needs to perform to rewrite according to interrupt request.
//      1.   Based on interrupt request of user program, change OnlyReti in the following interrupt vector table
//      2.   The interrupt name following the address in the corresponding vector table can be copied directly
//           For example, if wanting to use external interrupt0, OnlyReti in the corresponding interrupt table needs to be changed
// --------------------------------------------------------------
#pragma section const ADM_INT_VECTOR
void * const IntTbl1[] = {
    ADM_STARTUP,           /* 0x0000 : RESET
    SWI_IRQ,               /* 0x0002 : SWI_IRQ/INTUNDEF
    (void *)0xffff,        /* 0x0004 : Reserved
    WDT_IRQ,               /* 0x0006 : WDT_IRQ
    OnlyReti,              /* 0x0008 : TAMPER_IRQ
    OnlyReti,              /* 0x000A : CFD_IRQ
    OnlyReti,              /* 0x000C : Reserved
    U2A_IRQ,               /* 0x000E : U2A_IRQ/IntADM_Req
    OnlyReti,              /* 0x0010 : RTC IRQ
```

In the U2A interrupt service function, the command parameters placed in the shared SRAM memory under the USER mode can be read to determine which action to perform. In the meantime, the execution result will also be placed in the shared SRAM memory for the USER mode to read.

At the end of the U2A interrupt service function, there needs to be a jump back to USER mode program code to allow the microprocessor to return to USER mode.

USER Mode:

When the USER mode needs the service of the ADM mode, the parameters to be transmitted must be placed in the shared SRAM memory first, and then the ADM U2A interrupt is triggered by writing 0x5A 0x33 0x69 0xF3 to the MODEEXC register to switch to the ADM mode.


```
void  usrRequsetAdm()
{
    // Send data to Admin
    sendToAdmArray = ...;
    admc1Fun = ...;

    // Request Admin Service
    MODEEXC = 0x5A;
    MODEEXC = 0x33;
    MODEEXC = 0x69;
    MODEEXC = 0xF3;

    // Get Return data
    data[0] = recvFromAdmArray[0];
    ...
}
```
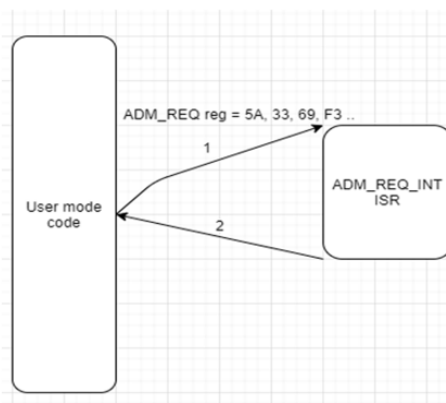
vii.　Others

Perform Admin debug password authentication in OCD, and do not set EEMC to Admin only.

Appendix D. Table of Terminology Abbreviation

D.1 Memory Related Terminology

Terminology Abbreviation	Definition
DMA	Direct Memory Access
EEPROM	Electrically-Erasable Programmable Read-Only Memory
FSR	Flash Status Register
I2C	Inter-Integrated Circuit
LEUART	Low Energy UART
MPU	Memory Protect Unit
PMR	Power Mode Register
RAM	Random Access Memory
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

D.2 Security Function Related Terminology

Terminology Abbreviation	Definition
AES	Advanced Encryption Standard
CRC	Cyclic Redundancy Check
DIC	Data Integrity Check
SHA	Secure Hash Algorithm
TRNG	True Random Number Generator

D.3 Function Related Terminology

Terminology Abbreviation	Definition
ADC	Analog to Digital Conversion
ALU	Arithmetic Logic Unit
BCD	Binary Coded Decimal
BROR	Brown Out Reset
DPA	Differential Power Analysis
DTM	Dead Time
DVO	Divider Output
GPRs	General Purpose Registers
HXTAL	High-speed External Clock
INTC	Interrupt Controller
KWU	Key Wake Up
LIRC	Low-speed Internal Reference Clock
LVD	Low Voltage Directive
LXTAL	Low-speed External Clock
PLL	Phase Locked Loop
PNIC	Peripheral Network Inter-Connect
POR	Power On Reset
PPG	Programmable Pulse Generator
PWM	Pulse Width Modulation
PxCFGCR	Pin Configuration Control Register
RTC	Real Time Clock

SPA	Simple Power Analysis
STM	Standard Timer Module
SWI	Software Interrupt
TBT	Time base timer
WDT	Watchdog Timer

Revision History

Version	Issued Date	Description
V1.2	2025/8/5	1. Sync with full datasheet V1.2
V1.1	2024/4/18	1. Sync with full datasheet V1.1
V1.0	2024/1/11	1. Sync with full datasheet V1.0
V0.7	2023/7/14	1. First version V0.7 issued