AP200301
SQ7617 EEPROM Programming Information
Ver. 1.0

Content

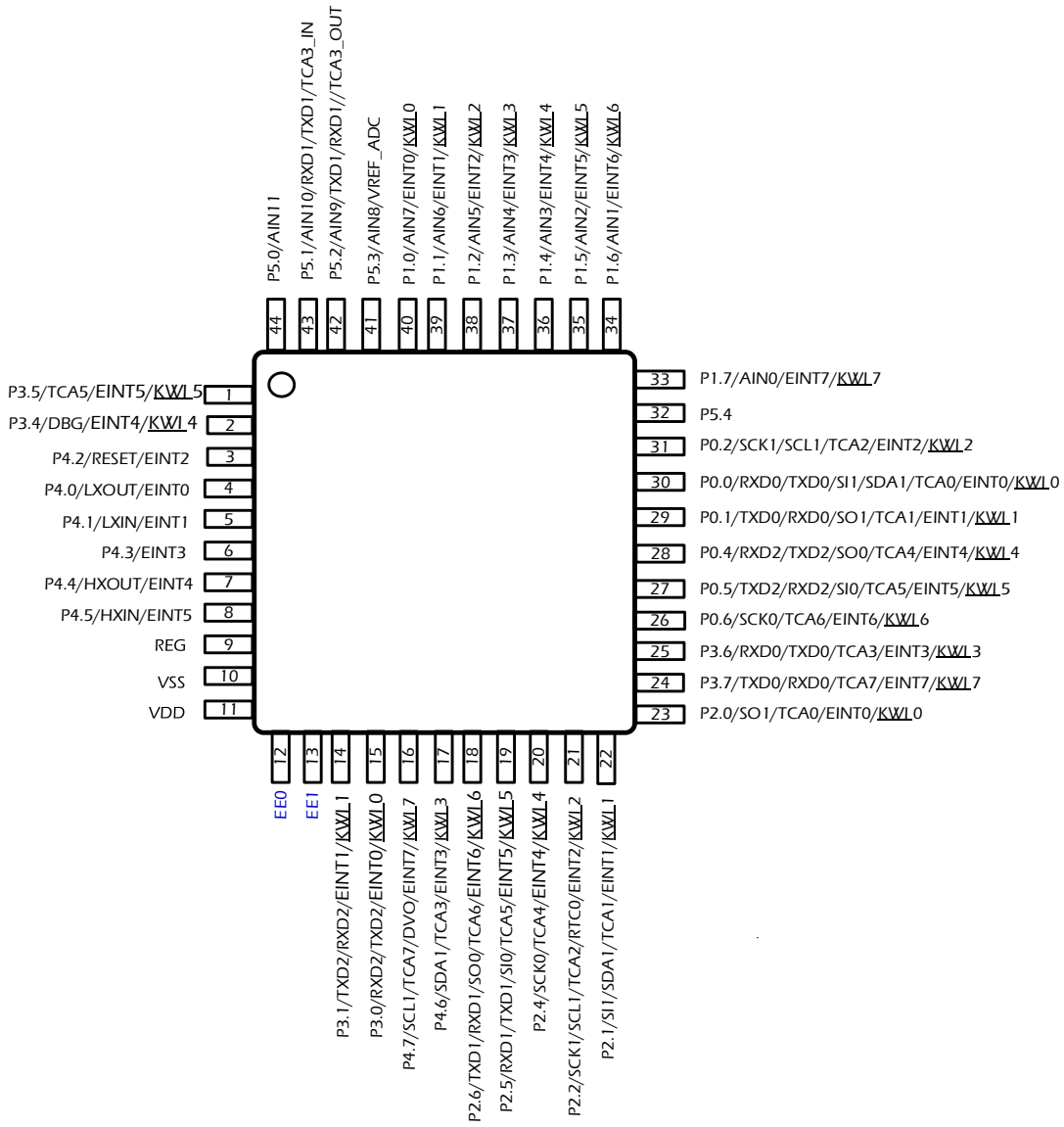
History

Version	Approved Date	Description
V1.0	2020/03/13	1st issued

1. Brief

SQ7617 provides 8K bytes of serial electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 words of 8 bits each.

2. Pin Description



The EEPROM operates as generic I2C slave device. When programming EEPROM, please connect to related pins as below:

Pin No.	Pin Name	Function
3	Reset	When programming EEPROM, please keep Reset as low-level . Recommend to connect to programmers' write protect pin.
10	VSS	GND
11	VDD	VDD
12	EE0	For EEPROM communication, SERIAL CLOCK (SCL). This pin is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device. The EEPROM operate as generic I2C slave device. Note1: This pin must connect to pull up 4.7kΩ. Note2: Because the device address is fixed at "1010000', only support one master to one slave.
13	EE1	For EEPROM communication, SERIAL DATA (SDA).This pin is bi-directional for serial data transfer. The EEPROM operate as generic I2C slave device. Note1: This pin must connect to pull up 4.7kΩ. Note2: Because the device address is fixed at "1010000', only support one master to one slave.

3. Memory Organization

SQ7617 has 8K bytes EEPROM: Internally organized as 256 pages of 32 bytes each. The 8K bytes EEPROM requires a 13-bit data word address for random word addressing. The device address is fixed at 1010000.

Device ADDR.	Page ADDR.	Byte Number		
		31	...	0
1010 000	0	Data Memory (256P x32B)		
	1			
	2			
	...			
	255			

4. Absolute Maximum Rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded and affect device reliability. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(V_{SS} = 0V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		-0.3 to 6.0	V
Input Voltage	V_{IN}	All I/O pins	-0.3 to VDD+0.3	V
Output Current (total)		All I/O pins	100	mA
Storage Temperature	T_{STG}		-50 to 125	℃

5. EEPROM DC Characteristics

The following defines the electrical characteristics of the device when it is operated at voltage and temperature maximum/minimum values. Unless otherwise stated, the standard conditions were determined at "operating temperature 25 ℃" .

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units.
Supply Voltage	V_{DD}		-	5.0	-	V
Supply Current	I_{DD1}	V_{DD}=5.0V, Read at 400KHz		0.4	1.0	mA
Supply Current	I_{DD2}	V_{DD}=5.0V, Write at 400KHz		2.0	3.0	mA
Input Low Level (Note)	V_{IL}		-0.6		V_{DD}x0.3	V
Input High Level (Note)	V_{IH}		V_{DD}x0.7		V_{DD}+0.5	V
Output Low Level1	V_{OL1}	V_{DD}=3.0V, I_{OL}=2.1mA			0.4	V

Note: V_{IL} min and V_{IH} max are reference only and are not tested.

6. EEPROM AC Characteristics

The following defines the electrical characteristics of the device when it is operated at voltage and temperature maximum/minimum values. Unless otherwise stated, the standard conditions were determined at "operating temperature 25 °C.

Parameter	Symbol	Min.	Max	Units.
Clock frequency, SCL	f_{SCL}		400	kHz
Clock pulse width low	t_{LOW}	1.3		us
Clock pulse width high	t_{HIGH}	0.6		us
Noise suppression time	t_1 (Note)		80	ns
Clock low to data out valid	t_{AA}	0.1	0.9	us
Time the bus must be free before a new transmission can start	t_{BUF} (Note)	1.3		us
Start hold time	$t_{HD,STA}$	0.6		us
Start setup time	$t_{SU,STA}$	0.6		us
Data in hold time	$t_{HD,DAT}$	0		us
Data in setup time	$t_{SU,DAT}$	100		ns
Inputs rise time	t_R		300	ns
Inputs fall time	t_F		300	ns
Stop setup time	$t_{SU,STO}$	0.6		us
Data out hold time	t_{DH}	100		ns
Write cycle time	t_{WR}		5	ms
Endurance (3.3V, 25℃, Page mode)			100,000	Write Cycles

Note 1: This parameter is characterized and is not 100% tested.

Note 2: AC measurement conditions:

RL (connects to V_{DD}) :pull up resistor 4.7 kΩ

Input pulse voltages : 0.3 V_{DD} to 0.7 V_{DD}

Input rise and fall times : ≦ 50ns

Input and output timing reference voltages : 0.5 V_{DD}

7. Device Operation

Clock and Data Transitions

The SDA pin is normally pulled high by an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode.

Acknowledge

All address and data words are serially transmitted to and from the EEPROM in 8-bbit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Memory RESET

After an interruption in protocol, power loss or system reset, the EEPROM can be reset in following steps:

1. Clock up to 9 cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

7-1 Bus Timing

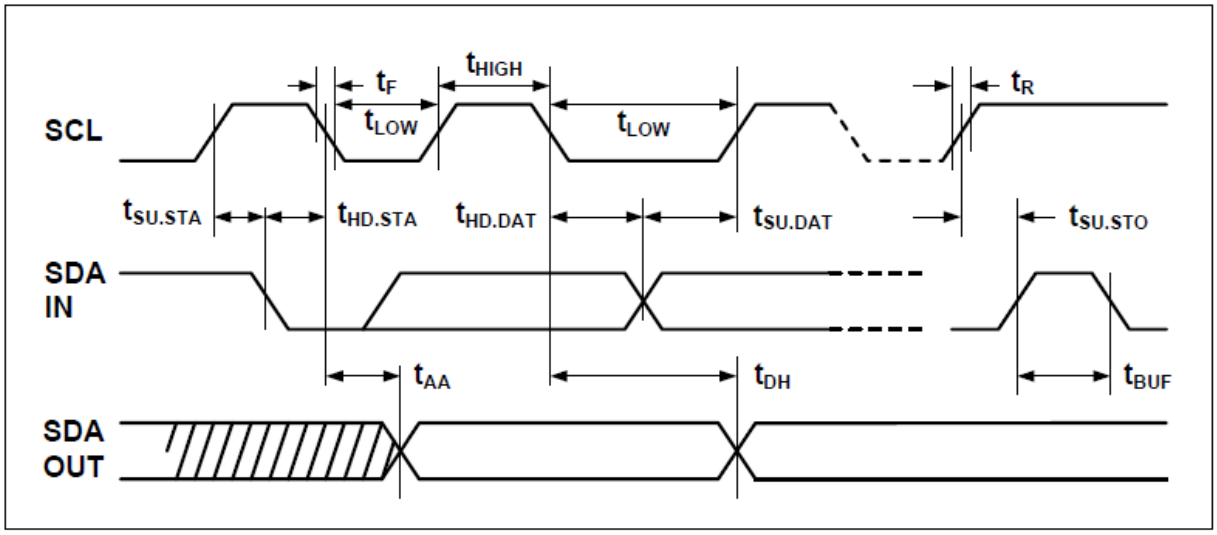


Figure 7-1 BUS Timing

7-2 Write Cycle Timing

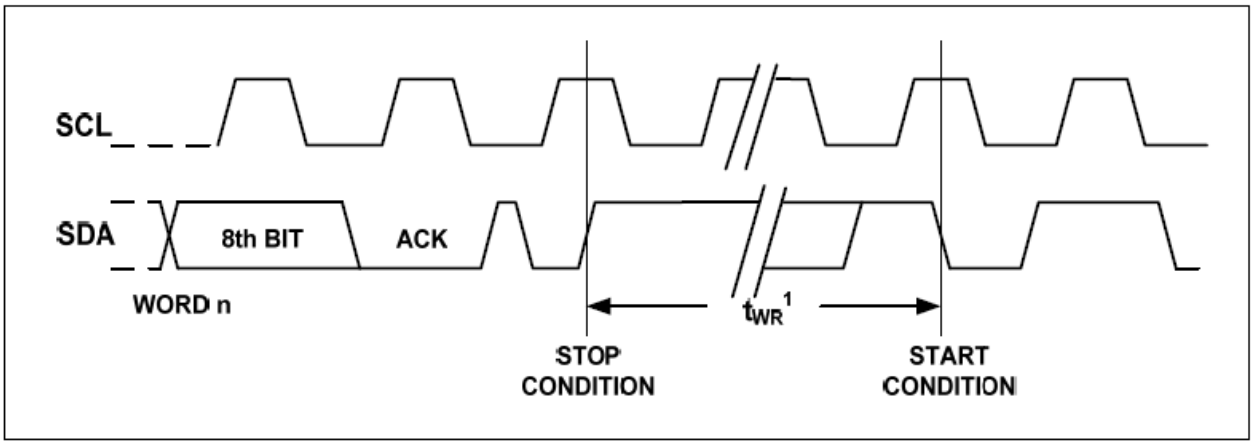


Figure 7-2 Write Cycle Timing

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

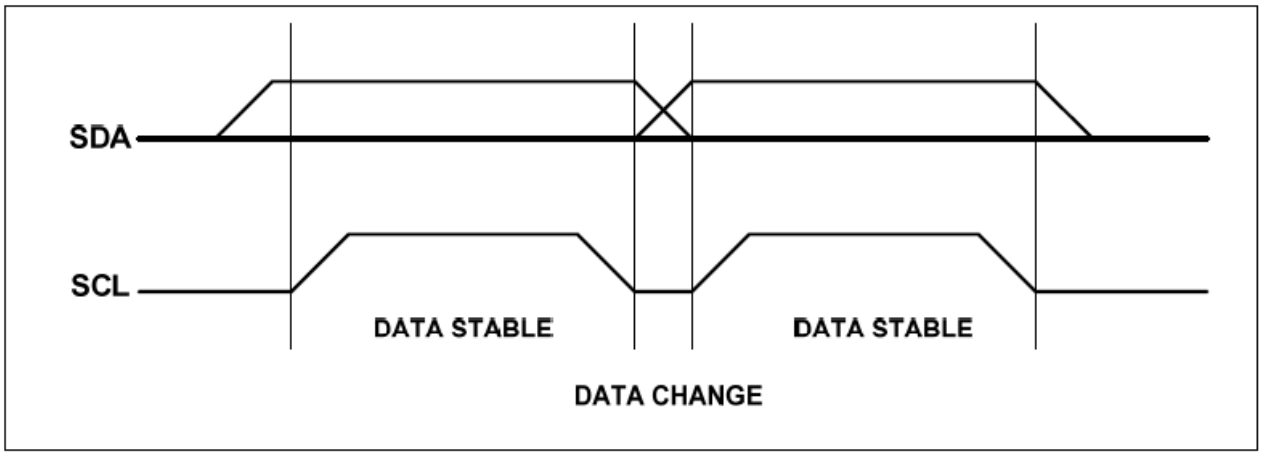


Figure 7-3 Data Validity

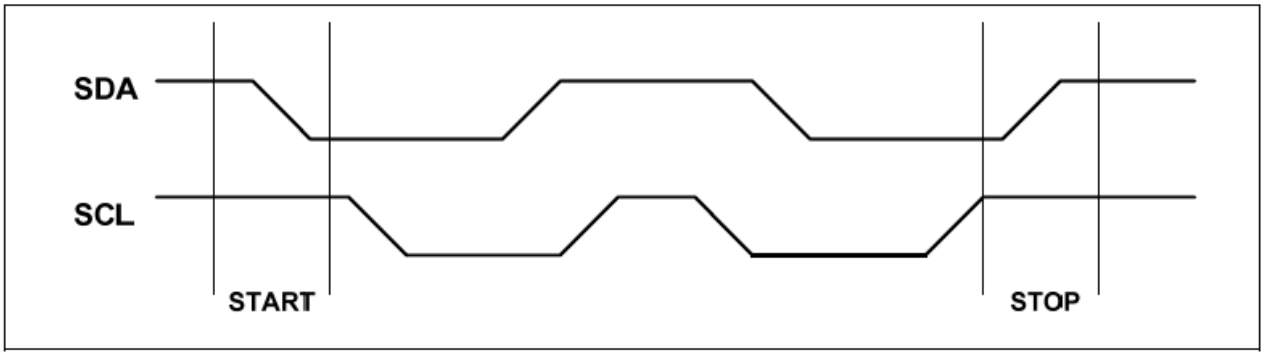


Figure 7-4 Start and Stop Definition

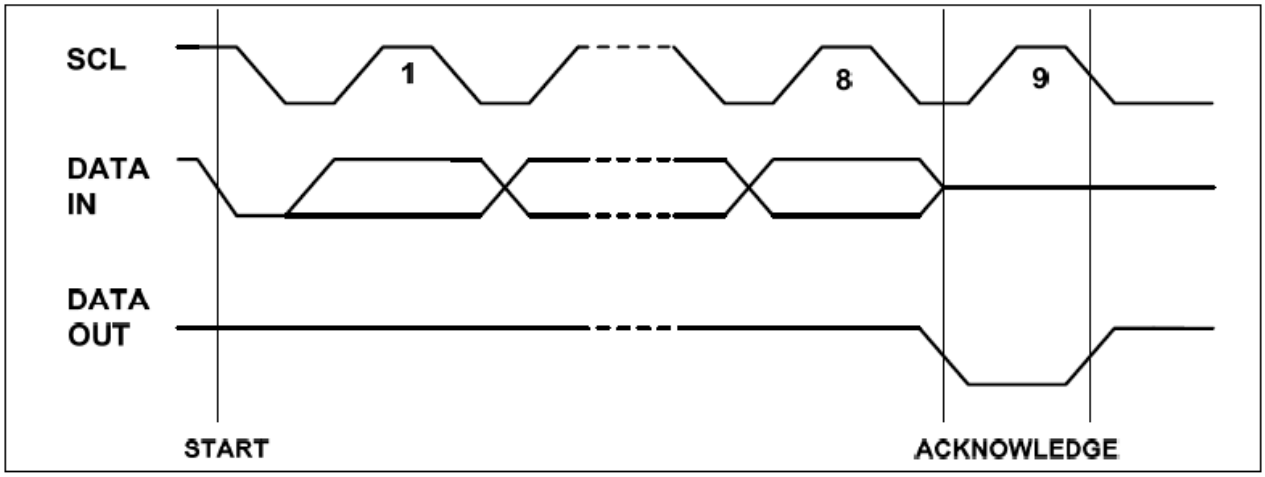


Figure 7-5 Output Acknowledge

8. Device Addressing

Data Memory Access

The 8K bytes EEPROM device requires a 8-it device address word following a start condition to enable the chip for a read or write operation.

The device address word consists of a mandatory 1010000 sequence for the first seven most significant bits.

The eight bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	0	0	0	R/W
	MSB							LSB

Table 8-1 Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	x	x	x	A12	A11	A10	A9	A8
	MSB							LSB

Table 8-2 First Word Address

Note: x= don't care.

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0

Table 8-3 Second Word Address

Note: x= don't care.

9. Write Operations

Byte Write

A write operation requires two 8-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} ,to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Page Write

EEPROM is capable of 32-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

The data word address lower seven bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data words are transmitted to the EEPROM, the data word address will "roll over", and previous data will be overwritten.

Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

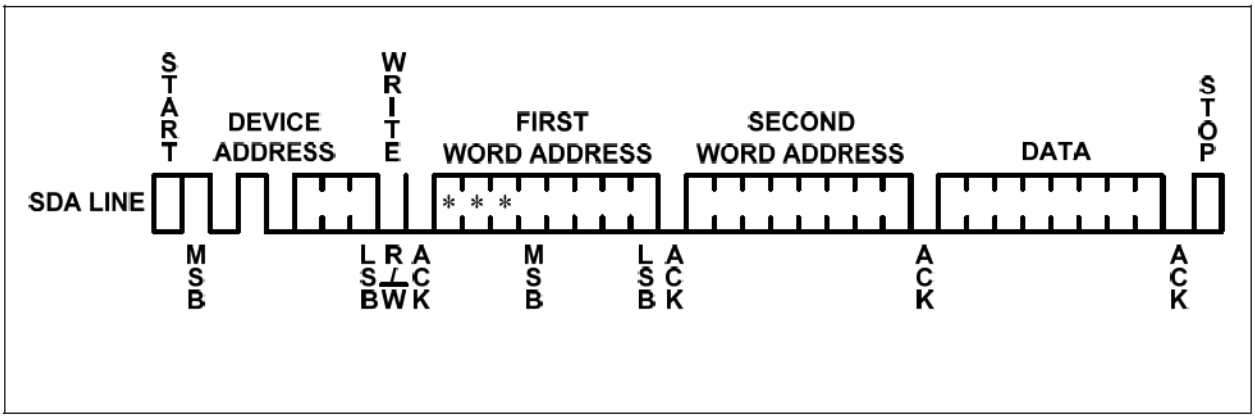


Figure 9-1 Byte Write

Note : *= don't care.

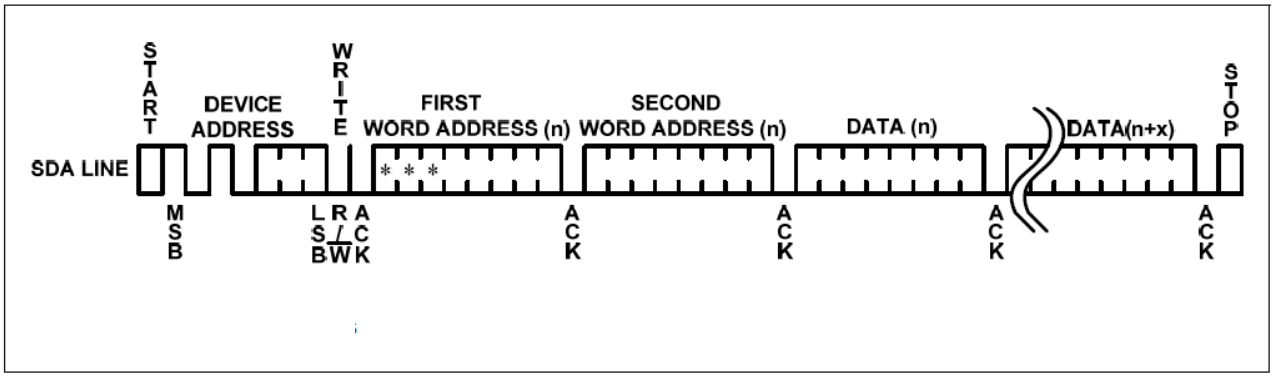


Figure 9-2 Page Write

Note : *= don't care.

10. Read Operations

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition.

Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition.

Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition.

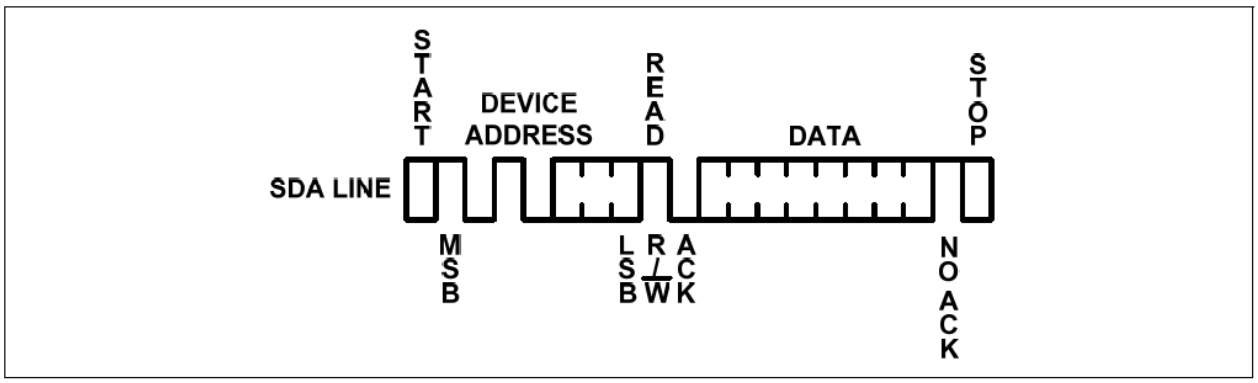


Figure 10-1 Current Address Read

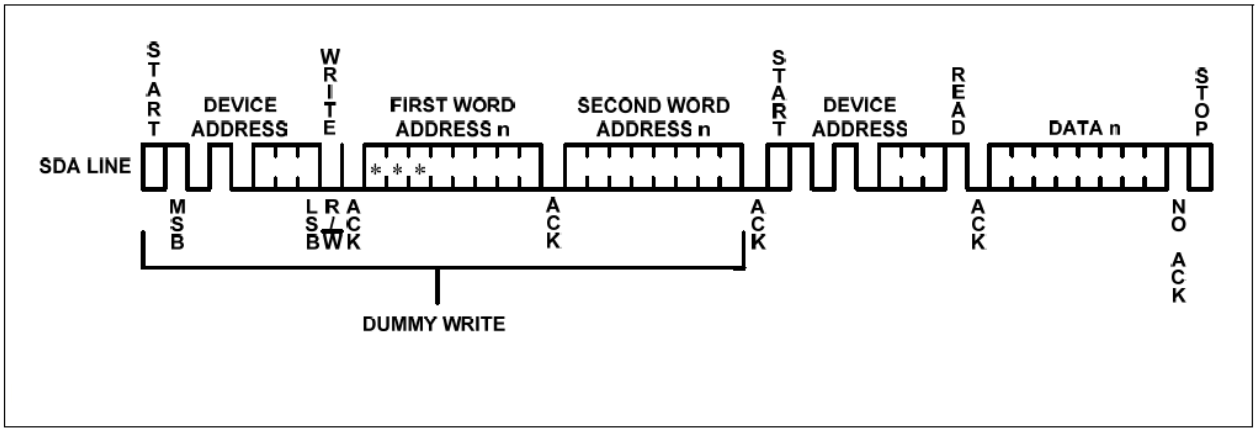


Figure 10-2 Random Read

Note : *= don't care.

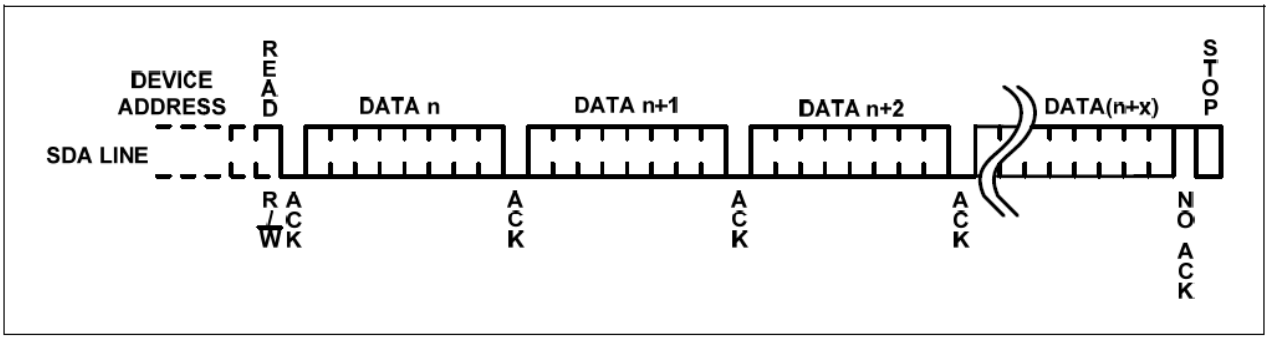


Figure 10-3 Sequential Read

11. How to Connect Programmer to a SQ7617

When using auto programmer to program the EEPROM, the specific pins on SQ7617 must be connected to the auto programmer system as shown below :

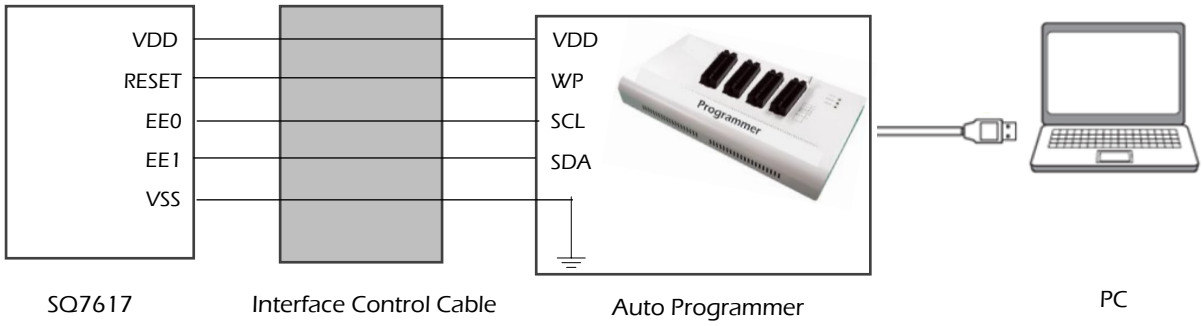


Figure 11-1

Note: The pin name of auto programmer may be different, detail please refer to the auto programmer manual.

Connection to Auto Programmer				
Pin Name		Input/ Output	Corresponding pin of auto programmer	Function
3	Reset	Input	Write protect pin	When programming EEPROM, please keep Reset as low-level. Recommend to connect to programmers' write protect pin.
10	VSS	GND	GND	0V
11	VDD	Power Supply	VDD	5V
12	EE0	Input	SCL	For EEPROM communication, SERIAL CLOCK (SCL). This pin must connect to pull up 4.7kΩ.
13	EE1	Input/ Output	SDA	For EEPROM communication, SERIAL DATA (SDA). This pin must connect to pull up 4.7kΩ.

Note 1 : Because the device address is fixed at "1010000', only support one master to one slave.